Switched-Mode Active Decoupling Capacitor Allowing Volume Reduction of the High-Voltage DC Filters

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***Abstract*—This paper describes active shunt LC decoupling circuit with ceramic capacitors, allowing volume reduction and lifetime improvement of the high-voltage dc filters. Active filtering is based on the energy exchange between high-voltage coupling and low-voltage auxiliary capacitors. The coupling capacitor enables use of the low-voltage switched-mode power stage and low-voltage auxiliary decoupling capacitor. Advantageously, this allows to reduce power dissipation, switching frequency ripple current, and to reduce volume of the circuit. Additionally, power efficiency and capacitor lifetime are improved by using recent high-voltage coupling multilayer ceramic capacitors, reaching very low *ESR*. This paper provides description of the active decoupling capacitor, and shows an example of the feedback control. Obtained performances are demonstrated on the prototype of 1300-μF/450-V capacitor, allowing to reduce volume by three, when compared to ordinary 450-V electrolytic capacitor.**

***Index Terms*—Active dc filter, active decoupling circuit, high-voltage decoupling with ceramic capacitors, photovoltaic decupling circuit, switched-mode decoupling circuit.**

I. Introduction

TYPICAL power electronic devices containing an ac–dc or dc–ac interface, such as the silicon-diode rectifier or dc–ac photovoltaic (PV) power inverter require bulky electrolytic decoupling (filtering) capacitors. These capacitors allow us to reduce ac voltage ripple on the dc power supply side, referred as input voltage V_{IN} in the following text. Reduction of the ac ripple voltage is essential for circuit operations and allows to improve the reliability, EMI quality, or acoustic interferences [1]. In PV applications, low ripple voltage allows efficient maximum power point tracking of the PV modules [2]. However, high-voltage (>300 V) applications require extremely bulky electrolytic capacitors, being typically dominant space-demanding components [3].

Decoupling of the dc input voltage is based on the charge transfer between the power source, tank capacitor, and load. Decoupling capacitor stores a *minimum charge* at the time of lowest terminal input voltage $V_{\mathrm{IN(min)}}$:

$$Q_{\min} = C_0 \cdot V_{\mathrm{IN(min)}} \tag{1}$$

Manuscript received June 23, 2015; revised September 7, 2015; accepted October 21, 2015. Recommended for publication by Associate Editor H. Wang.

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Digital Object Identifier 10.1109/TPEL.2015.2500920

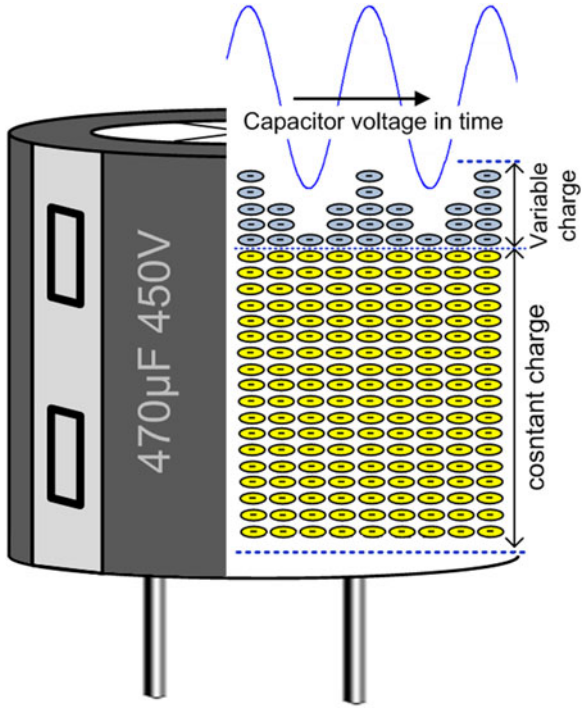

Fig. 1. Inefficient use of the high-voltage electrolytic capacitor. Capacitor contains large constant charge $Q_{\min}$ and small variable charge ΔQ.

and similarly, contains *maximal charge* at the positive peak of the input voltage:

$$Q_{\max} = Q_{\min} + \Delta Q = C_0 \cdot V_{\mathrm{IN(min)}} + C_0 \cdot \Delta V_{\mathrm{IN}}. \tag{2}$$

Here, ΔQ is *variable charge* related to the peak-to-peak input ac voltage ΔV_{IN}. It results, that high-voltage decoupling capacitor typically stores large "*constant*" charge $Q_{\min}$ and small variable charge ΔQ, creating *filtering current* I_{C0}. As illustrated in Fig. 1, this leads to an inefficient use of the capacitor dielectric.

Besides low filtering efficiency, electrolytic capacitors exhibit short lifetime, typically in order of several thousands of hours. The lifetime is reduced namely under high ac ripple current and high temperature conditions. Regarding this limitation, active decoupling circuits based on high-voltage film capacitors were presented. These circuits aim to increase the low value of the film-capacitor by various switched-mode approaches. As an example, flyback [4] or push-pull [5] power stages use high-voltage decoupling film capacitors, acting as additional energy storage device.

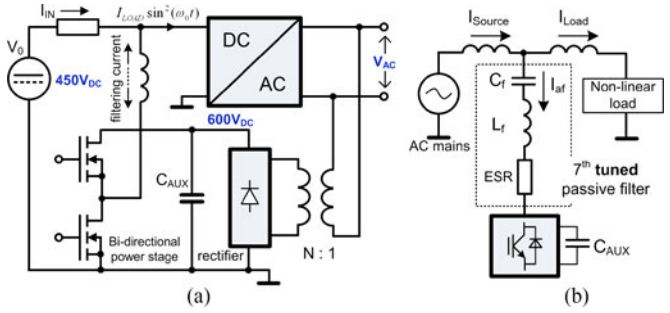

Fig. 2. Parallel active decoupling circuit [6], [7] with high-voltage power stage, decoupling capacitor, and 600 V dc voltage source, b) hybrid shunt active LC power filter [9], [10] used for power conditioning.

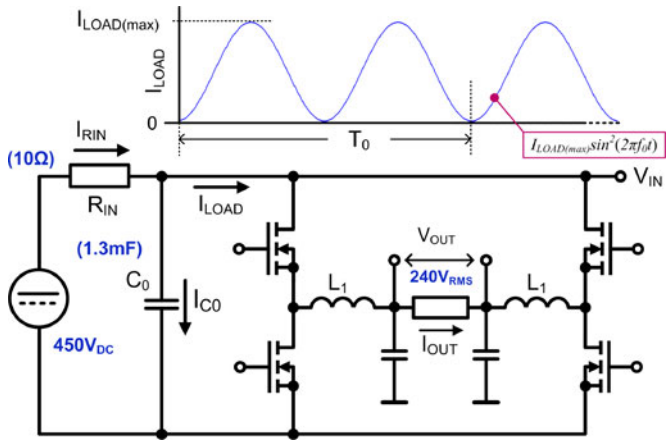

Fig. 3. High-voltage nonisolated full-bridge power inverter creating input voltage ($V_{\rm IN}$) ripple on the dc source input resistance $R_{\rm IN}$ and decoupling capacitor C_0.

A parallel active filtering circuit Fig. 2(a) is presented in [6] or [7]. This circuit contains a bidirectional power stage creating power-link between the dc-line $V_{\rm IN}$ and high-voltage auxiliary (decoupling) capacitor. Compared to Fig. 1, this decoupling capacitor is allowed to operate under large ripple voltage ΔV, allowing more efficient utilization of the dielectric. In order to enable the buck-mode operation, the power stage operates under voltage higher than dc-link voltage, e.g., $\sim$ 600 V for $V_{\rm IN(DC)} = 400$ V. This voltage is obtained by a transformer–rectifier 600-V dc source shown in Fig. 2(a). Due to this very high voltage, power-switches and inductor have similar maximal ratings, compared to main power stage of the power inverter [8].

Hybrid shunt LC active power filtering (APF) is a widely used technique designed to eliminate the harmonic currents from the ac distribution networks [9], [10]. As shown in example Fig. 2(b), the power stage is connected to one (or more) passive LC filters, tuned to a particular ac-line harmonic. The power stage produces harmonic current, which is equal in magnitude but has opposite phase to the unwanted harmonic currents presented in the grid. Similarly to Fig. 2(a), the active buffer is decoupled by an auxiliary capacitor $C_{\rm AUX}$. As mentioned e.g., in [9], C_f enables to decrease the maximum ratings of the power stage, which allows to reduce the dissipated power and implementation volume of the APF.

An example of the decoupling circuit used also in following mathematical demonstration is shown in Fig. 3. This figure represents an input part of H-Bridge dc–ac power inverter [11], transforming the high input voltage 450 $V_{\rm DC}$ to 240 $V_{\rm RMS}$ ac output voltage. The 450-V dc source V_0 (e.g., PV panel) contains an internal resistance $R_{\rm IN}$, and high-voltage large-value decoupling capacitor C_0.

Applying appropriate sinusoidal pulse-width modulation (PWM) modulation to the transistors allows us to generate output sinewave voltage $V_{\rm OUT}$. The output power $V_{\rm OUT} \cdot I_{\rm OUT}$ creates a load current $I_{\rm LOAD}$, being typically in form of a squared sinewave:

$$I_{\rm LOAD}\,(t) \cong I_{\rm LOAD(max)} \sin^2(\omega_0 t). \tag{3}$$

It results that the load current fundamental frequency is twice the output voltage frequency f_0, i.e., $f(I_{\rm LOAD}) = 2{\cdot}f_0$. The magnitude of the Fourier series coefficients can be obtained by using trigonometric identity:

$$A_0 \sin^2(x) = \frac{A_0}{2} - \frac{A_0}{2}\cos(2x)\,. \tag{4}$$

Consequently, average dc load current $I_{\rm LOAD(DC)} = 1/2 \cdot I_{\rm LOAD(max)}$, and $2f_0$ load current $I_{\rm LOAD(peak-to-peak)} = I_{\rm LOAD(max)}$. The input voltage $\Delta V_{\rm IN}$ therefore contains dominant single-tone component $2f_0$ of amplitude:

$$V_{\rm IN(peak-to-peak)} \cong I_{\rm LOAD(max)} \cdot |Z_{\rm IN}| \tag{5}$$

where, $Z_{\rm IN}$ is the parallel connection of $R_{\rm IN}//C_0$ at $2f_0$.

As an example, $P_{\rm OUT} = 2$ kW power inverter from Fig. 3 requires $\approx$ 1300-μF/450-V capacitor, in order to obtain $10V_{\rm peak-to-peak}$ input ripple voltage. This capacitor drives $\approx 10A_{\rm peak-to-peak}$ ac current, and fits in $\approx$ 130 cm^3.

In the following text, approach allowing us to reduce volume and increase the reliability of the high-voltage filtering capacitors is described. The concept of the series LC shunt decoupling circuit is described in Section II. Section III presents analysis of the power losses of dominant passive components, and explains the choice and advantages of low-ESR multilayer ceramic capacitor (MLCC) C_T and $C_{\rm AUX}$. Section IV illustrates the example of the feedback control scheme, whereas practical realization and measured results are presented in Section V.

II. Active DC Decoupling Capacitor

For given frequency ω, the capacitor "filtering" current $I_{C0}(\omega)$ can be expressed as

$$I_{C0} = j\omega\, C_0 V_{\rm IN} \tag{6}$$

where $V_{\rm IN}$ is the RMS voltage resulting from (5). It follows that beyond the increase of capacitor value, current I_{C0} can be increased by amplifying the capacitor terminal ac voltage. This approach is used in low-power analog circuits such as active frequency filters, or Miller-type frequency compensation of operational amplifiers [12]–[14]. Circuit allowing to increase the capacitor ac voltage $V_{\rm CT}$ is shown in Fig. 4.

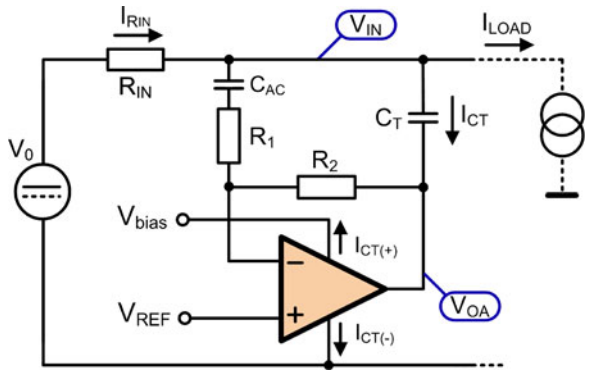

Fig. 4. Active capacitor with operational amplifier.

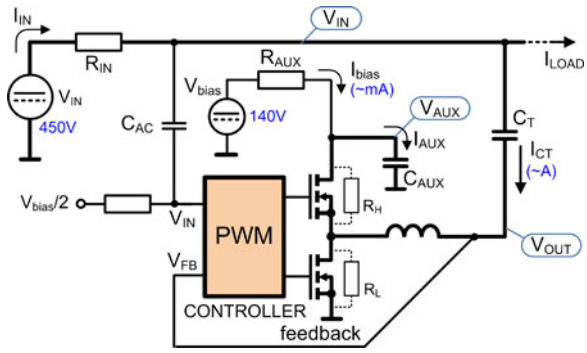

Fig. 5. Idealized schematic of the high-power active decoupling capacitor allowing low (middle)-voltage operation of the power-stage.

This circuit contains a power operational amplifier mounted as inverter, high-voltage coupling and filtering (tank) capacitors $C_{\rm AC}$ and C_T, and feedback resistors R_1 and R_2. Advantageously, high-voltage coupling and filtering capacitors enable low/middle voltage operations of the amplifier. The amplifier output voltage $V_{\rm OA}$ is given as:

$$V_{OA} = -\frac{R_2}{R_1} V_{\rm IN} = -G_0 \cdot V_{\rm IN} \tag{7}$$

where impedance of coupling capacitor is neglected. Since $V_{\rm OA}$ is applied on the bottom terminal of C_T, capacitor drives high filtering current I_{CT}:

$$I_{CT} = j\omega\,(1+G_0)\,C_T V_{\rm IN}. \tag{8}$$

In order to obtain identical filtering current compared to the standalone capacitor C_0 in Fig. 3, (6), value of C_T in Fig. 4 can be reduced by $(1 + G_0)$, or

$$C_T = \frac{C_0}{(1+G_0)}. \tag{9}$$

A. Switched-Mode Power Amplifier

As shown in Fig. 4, high tank-capacitor current $I_{\rm CT}$ is delivered by the operational amplifier output $V_{\rm OA}$. However, this current produces significant power losses in the amplifier output stage. Moreover, during the negative period of $V_{\rm OUT}$, $I_{\rm CT}$ is absorbed by the ground terminal, whereas during the positive period of $V_{\rm OUT}$, the output current is delivered by the power supply rail $V_{\rm bias}$. Beyond the needs for a high-current amplifier power supply, the losses occurring in the amplifier power stage render the concept inefficient.

It is therefore convenient to replace the operational amplifier by an autonomous circuit, achieving very-low power dissipation. Similarly to the concepts shown in Fig. 2, this can be obtained by employing switched-mode power stage shown in Fig. 5. This power stage is powered from a low-voltage decupling (tank) capacitor $C_{\rm AUX}$. In contrast to the high-voltage transformer by shown in Fig. 2(a), dc bias current $I_{\rm bias}$ is delivered via low-power (<0.5 W) auxiliary resistance $R_{\rm AUX}$. Resistance $R_{\rm AUX}$ allows us to attenuate residual $2f_0$ and $4f_0$ ac components from $I_{\rm AUX}$ (see Section III. (C), which allows us to reduce ac power losses in $V_{\rm bias}$. The value of $V_{\rm bias}$ is designed to maintain $V_{\rm AUX}$ higher than $V_{\rm OUT}$ (buck-mode operation) with sufficient margin.

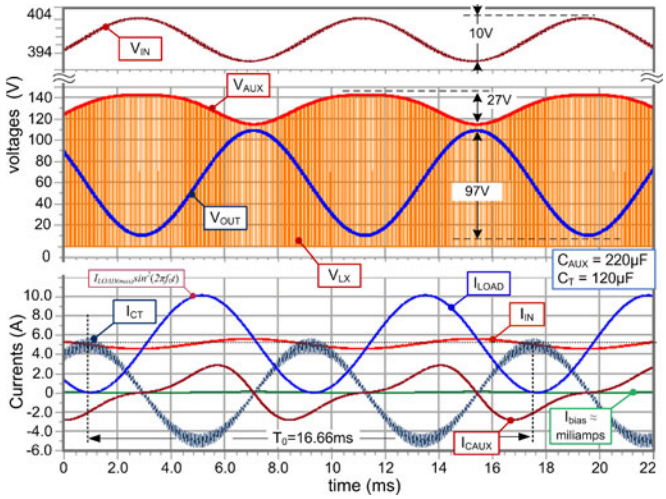

Fig. 6. Idealized simulation of the switched-mode active capacitor from Fig. 5. Simulation was provided on switched-mode model, except $I_{\rm CAUX}$ extracted from linearized model Fig. 7. Simulation parameters were $C_T = 120\ \mu$F, G$_0$ = 10, $V_{\rm IN} = 450$ V, $R_{IN} = 10\Omega$, $V_{\rm bias} = 140$ V, $R_{\rm bias} = 220\Omega$, $C_0 = 50\ \mu$F and $ESR_{\rm CT} = 500$ mΩ.

Similarly to the linear implementation shown in Fig. 4, the switched-mode power stage delivers a high output current $I_{\rm CT}$ to the capacitor C_T. Thanks to the absence of resistive elements, the power dissipated in the power stage is ideally zero.

The circuit operations are demonstrated by the ideal switched-mode simulation in Fig. 6. Here, we notice namely the high tank capacitor current $I_{\rm CT}$. This current is allowed thanks to the energy exchange between the auxiliary and tank capacitors $C_{\rm AUX}$ and C_T. During the positive half-period of $V_{\rm OUT}$, the tank capacitor C_T is discharged, causing the voltage $V_{\rm AUX}$ to decrease. Similarly, when the output voltage $V_{\rm OUT}$ decreases, the tank capacitor voltage increases simultaneously with auxiliary voltage $V_{\rm AUX}$. The small dc bias current $I_{\rm bias}$ is therefore only due to the inevitable ohmic and dynamic power losses occurring in the switched-mode power stage and LC filter (see Section III). Roughly, this current can be in order of tens of mA for the output current $I_{\rm CT}$ being several Amps. In the circuit

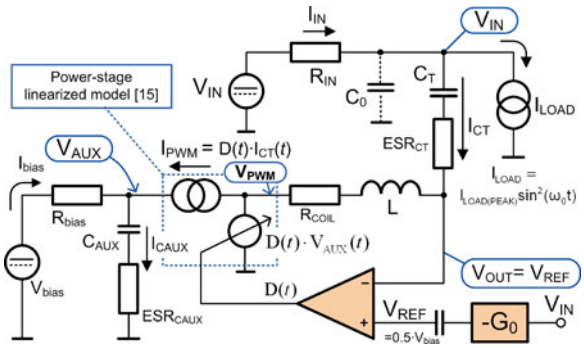

Fig. 7. Large signal linearized model of Fig. 5 active capacitor.

shown in Fig. 5, the control law produces the output ac voltage $V_{\rm OUT} = -G_0 \cdot V_{\rm IN}$ with a dc component $V_{\rm OUT(DC)} = V_{\rm bias}/2$.

B. Input Bias Current $I_{\rm bias}$

The power $P_{\rm loss}$ dissipated during the circuit operation is delivered by the auxiliary voltage source $V_{\rm bias}$. As already mentioned, the dissipated power is zero when considering ideal components in $I_{\rm CT}$ current path. This can be shown by the steady-state analysis of linearized model shown in Fig. 7. Here, the power stage was linearized by using technique described in [15].

The average value of $I_{\rm PWM}(t)$ corresponds to the dc bias current $I_{\rm bias}$. For the excitation $2f_0$, $V_{\rm IN}(t)$ results in

$$V_{\rm IN}\,(t) = |Z_{\rm IN}| \cdot I_{\rm LOAD}\,(t) = V_{\rm IN(max)} \sin\,(2\omega_0 t) \qquad (10)$$

where $Z_{\rm IN}$ is the input impedance $R_{\rm IN}//C'_T$ and $C'_T = (1+G_0)\,C_T$ is the equivalent capacitance of the active capacitor.

While capacitor voltage is $V_{\rm CT}(t) = (1+G_0)\,V_{\rm IN}\,(t)$, capacitor current can be expressed as

$$I_{\rm CT}\,(t) = C_T \frac{dV_{\rm CT}\,(t)}{dt} = \underbrace{2\omega_0 C'_T V_{\rm IN(max)}}_{ICT(\max)} \cos\,(2\omega_0 t)\,. \qquad (11)$$

At low frequency, $V_{\rm PWM}(t)$ and $V_{\rm OUT}(t)$ can be assumed equal, i.e., $V_{\rm PWM} \cong V_{\rm OUT} = -G_0 V_{\rm IN}$. The output voltage $V_{\rm PWM} = {}_{\rm AUX}\,(t) D(t)$ can then be written as

$$V_{\rm AUX}\,(t)\,D\,(t) = \frac{V_{\rm AUX}\,(t)}{2} - G_0 V_{\rm IN}\,(t) \qquad (12)$$

which yields the duty-cycle

$$D\,(t) = \frac{1}{2} - \frac{G_0 V_{\rm IN}\,(t)}{V_{\rm AUX}\,(t)}. \qquad (13)$$

Input current $I_{\rm PWM}\,(t) = D\,(t)\,I_{\rm CT}\,(t)$ can be expressed by (11) and (13)

$$D\,(t)\,I_{\rm CT}\,(t) = I_{\rm CT(max)} \cos\,(2\omega_0 t) \left(\frac{1}{2} - \frac{G_0 V_{\rm IN(max)} \sin\,(2\omega_0 t)}{V_{\rm AUX}(t)}\right) \qquad (14)$$

and integrated over one conduction cycle $T_0 = 1/f_0$

$$I_{\rm PWM}({\rm DC}) = \frac{1}{T_0}\int_0^{T_0} D\,(t)\,I_{\rm CT}\,(t)\,dt = 0. \qquad (15)$$

Equation (15) signifies that use of ideal (lossless) power stage results in zero power loss and zero dc current delivered by external voltage source $V_{\rm bias}$.

III. Power Efficiency Consideration

Presented decoupling circuit aims to compensate for fast current fluctuations in the decoupled dc-line. Accordingly, the power losses occurring in the decoupling circuit are load-dependent. Similarly to standard dc–dc converter, the power losses are dominated by the dynamic power at low output current, and by the conductive ohmic power when circuit compensates high load current [16]. The high-output power dissipation also includes a nonnegligible magnetic core loss. Regarding the low required device volume, reduced dissipation at high output power allows us to considerably reduce the volume of the heat-sink.

A. Power-Loss Distribution

While switching CV^2f and nonoverlapping dynamic power can be reduced by appropriate choice of frequency $f_{\rm sw}$ and power transistors, the reduction of ohmic losses is limited by low required volume of the passive components. Parasitic resistance encountered in $I_{\rm CT}$ current path can be given as a sum of elements shown in Figs. 5 and 7:

$$R_{I_{\rm CT}} = \underbrace{D \cdot R_H + (1-D)\,R_L}_{R_{\rm MOS}} + R_{\rm COIL} + ESR_{\rm CT} + k \cdot ESR_{CAUX} \qquad (16)$$

where k is duty-cycle dependent constant $k \approx$ ½ discussed later, and $R_{H,L}$ are the on-resistance of related transistors.

While ac RMS current $I_{\rm CT}$ is almost equal to ac RMS current of $I_{\rm LOAD}$ (see Fig. 7), the resistive dissipated power can be expressed as

$$P_{\rm JOULE} \cong R_{I_{\rm CT}} \cdot I^2_{\rm LOAD(RMS\_AC)}. \qquad (17)$$

When considering fundamental frequency $2f_0$ = 100/120 Hz (4), the output RMS current results as

$$I_{CT(\rm RMS)} \cong \frac{I_{\rm LOAD(max)}}{2\sqrt{2}}. \qquad (18)$$

As already mentioned, the power dissipated on the parasitic elements (16) is to be supplied by $V_{\rm bias}$. Power $V_{\rm bias} \cdot I_{\rm bias}$ is therefore equal to (17) which yields

$$I_{\rm bias} = \frac{R_{I_{\rm CT}} I^2_{CT(\rm RMS)}}{V_{\rm bias}}. \qquad (19)$$

The available power-MOSFETs reach $R_{\rm DS(ON)}$ of tens of mΩ ($V_{\rm DSS} = 150$ V), whereas the power-inductors with adequate saturation current reach $R_{\rm COIL}$ of ≈ 300 mΩ. Unfortunately, high-voltage electrolytic capacitors reach $ESR_{\rm CT}$ in order of unit of ohms. This causes electrolytic C_T to be a dominant

contributor regarding the power loss (see fabricant references, e.g., [17]). Moreover, electrolytic capacitors operating under high ac current suffer from overheating, resulting in accelerated aging [17]–[19].

As an example, Fig. 5 decoupling circuit operating with 2-kW power inverter use electrolytic capacitor $C_T = 120\ \mu$F with *ESR* $= 1.5\ \Omega$. While driven by $I_{CT(\mathrm{RMS})} = 3.4$ A, this capacitor dissipate $P_{\mathrm{JOULE}} = 17$ W (see Fig. 6) which requires $I_{\mathrm{bias(DC)}} = 120$ mA at $V_{\mathrm{bias}} = 140$ V. By using low-*ESR* 0.5-Ω capacitor, I_{bias} can be reduced to 40 mA ($P_{\mathrm{JOULE}} = 5.6$ W). While considering 2 kW inverter and $I_{CT(\mathrm{peak-to-peak})} = 9.6$A, $I_{\mathrm{bias}} = 40$ mA is acceptable, but renders the electrolytic coupling capacitor C_T dominant contributor from (16).

B. MLC Ceramic Coupling Capacitor C_T

The physical origin of the power loss occurring in the coupling capacitor C_T appears from the linearized model shown in Fig. 7. When considering $V_{\mathrm{OUT}} = V_{\mathrm{REF}}$ and fundamental frequency $2\omega_0$ (see (4)), parasitic resistance ESR_{CT} introduces a phase shift between $I_{\mathrm{CT}}(t)$ and $V_{\mathrm{OUT}}(t)$

$$\varphi = -\tan^{-1}\left(2\omega_0 ESR_{\mathrm{CT}} C_T\right). \tag{20}$$

Power stage input current $I_{\mathrm{PWM}}(t) = D(t)\, I_{\mathrm{CT}}(t)$ can be expressed from (14) as

$$I_{\mathrm{PWM}}(t) = I_{\mathrm{CT(max)}}\cos\left(2\omega_0 t + \varphi\right) \left(\frac{1}{2} - \frac{G_0 V_{\mathrm{IN(max)}}\sin\left(2\omega_0 t\right)}{V_{\mathrm{AUX}}(t)}\right). \tag{21}$$

By integration over one period ($1/T_0 = 50/60$ Hz)

$$\frac{1}{T}\int_0^{T_0} \sin(2\omega_0 t)\cdot\cos(2\omega_0 t + \varphi)dt = -0.5\cdot\sin(\varphi). \tag{22}$$

DC bias current value then depends on the phase shift φ

$$I_{\mathrm{bias(DC)}} = \frac{\omega_0 C_T' V_{\mathrm{IN(max)}}^2 G_0}{V_{\mathrm{bias}}}\cdot\sin(\varphi). \tag{23}$$

In this equation, $V_{\mathrm{AUX}}(t)$ was considered constant, i.e., $V_{\mathrm{AUX}}(t) = V_{\mathrm{bias}}$. As an example, using high-quality electrolytic capacitor 120 μF with $ESR_{\mathrm{CT}} = 0.5\ \Omega$ creates phase shift $\varphi = -2.6°$ ($2f_0 = 120$ Hz). Integral (23) yields $I_{\mathrm{bias(DC)}} = 40$ mA ($V_{\mathrm{IN(max)}} = 5$ V 120 Hz), which corresponds to (19).

Recent progress in the fabrication of MLCC allows us to obtain high-density and high-breakdown voltage capacitors of units of μF for ~500 V [20]. These capacitors offer very-low ESR compared to their electrolytic counterparts. Moreover, thanks to the absence of continuous evaporation of the dielectric occurring in electrolytic capacitors, MLCC offers theoretically unlimited lifetime. On the contrary, X7T dielectric exhibits high (over 50%) permittivity drop, resulting in capacitance decrease for high bias voltages. Example of measured bias characteristic is shown in Fig. 8, or in fabricant references [20] and [21].

In order to overcome the dc-bias dependence of X7T dielectric, 120-μF 400-V capacitor was realized by a set of 160 pieces of 2.2-μF/450-V ceramic capacitors. This assembly reached 9.7 cm^3 rectangular volume (see Fig. 16). (*note*: ceramic capacitor packs [21] are also available in the market). The low-voltage

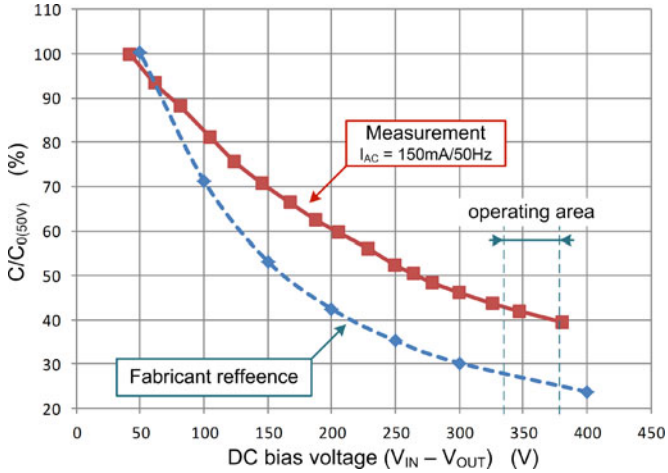

Fig. 8. Relative bias-voltage capacitance variation of the high-voltage MLCC. Measurement provided for ~150 mA ac current. Comparison refers to [20] 2.2 μF/450V X7T MLCC.

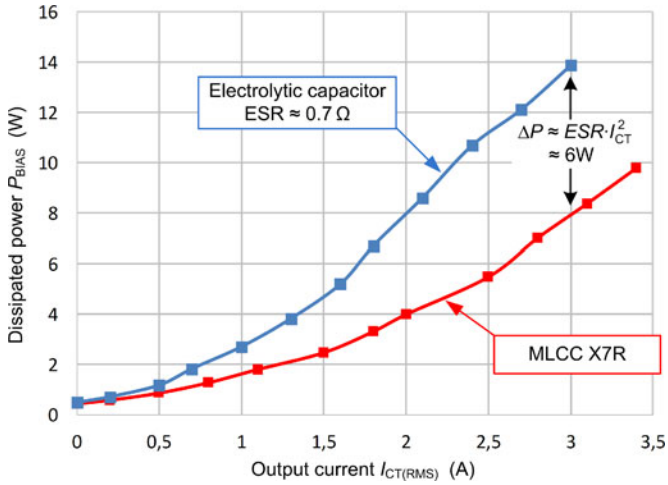

Fig. 9. Measured power $V_{\mathrm{bias}} \cdot I_{\mathrm{bias}}$ of decoupling circuit with ceramic and electrolytic capacitor C_T ($V_{\mathrm{bias}} = 150$ V).

measurements of this capacitor showed ESR = 50 mΩ 120 Hz. By employing analysis presented in previous paragraph, the power consumption related to C_T decreased to $I_{\mathrm{bias}} = 5$ mA only (~0.5 W).

Comparison of the power dissipation obtained with ceramic and electrolytic capacitors C_T is shown in Fig. 9. During the operation, excessive heat of the electrolytic capacitor was observed under high I_{CT}. Remaining power dissipation is caused by the losses of power stage, inductor, and ESR_{CAUX}.

It is worth to mention that standalone electrolytic capacitor of $(1 + G_0)\cdot C_T = 1300\ \mu$F reaches ESR of $\approx$ 150 mΩ at 120 Hz, which results in ~1.5 W power loss.

C. Auxiliary Capacitor ESR_{AUX}

Auxiliary capacitor acts as energy buffer, allowing us to absorb or deliver the power stage output current. Its value is designed to be larger than C_T, but exhibits lower charge variation ΔQ. Thanks to the coupling capacitor C_T, maximum voltage

of C_{AUX} is reduced. This enables to use high density (low volume) component. When compared to C_T, RMS current of C_{AUX} is lower, but still requires judicious selection of the capacitor dielectric.

I_{CAUX} delivered from model Fig. 7 is given by (14), and its example is plotted in Fig. 6 (by means of linearized model). Equation (14) can be rearranged as

$$I_{\mathrm{CAUX}}(t) = \frac{1}{2} I_{\mathrm{CT}}(t) - \frac{V_{\mathrm{OUT}}(t) \cdot I_{\mathrm{CT}}(t)}{V_{\mathrm{AUX}}(t)} \tag{24}$$

where term ½ corresponds to dc operating point (13). Equation (24) can be developed as

$$I_{CAUX}(t) = \frac{I_{CT(\max)}}{2} \cos(2\omega_0 t) - \frac{\alpha \sin(2\omega_0 t)\cos(2\omega_0 t)}{V_{AUX}(t)} \tag{25}$$

where α substitutes $I_{CT(\max)} \cdot G_0 \cdot V_{\mathrm{IN}(\max)}$ term from (14). It results that auxiliary capacitor current I_{CAUX} contains constant part $1/2 I_{\mathrm{CT}}(2\omega_0)$ of the power-stage output current, and also double frequency component $4\omega_0$. Magnitude of this second term can be controlled *via* dc voltage V_{AUX}.

As shown by (16), ESR_{CAUX} creates additional high-current power loss. Use of low ESR (ceramic) capacitors C_{AUX} therefore allows us to maintain very low power dissipation and high lifetime of the decoupling circuit. However, use of electrolytic aluminum capacitors can be envisaged thanks to reduced capacitor ripple current. Moreover, capacitors of higher value usually reach proportionally lower *ESR*. Both these parameters result in decreased dissipated power RI^2, and consequently increased lifetime. For illustration, capacitor value used in the prototype is $C_{\mathrm{AUX}} \approx 2C_T$. This corresponds approximately to $ESR_{\mathrm{CAUX}} = 1/2 ESR_{\mathrm{CT}}$, when considering C_T being also electrolytic capacitor. As described in [18], the reduction of the dissipated heat has dominant impact on capacitor lifetime and allows, in some applications, a reliable use of the aluminum electrolytic capacitors.

IV. Linear Feedback Controller

The aim of the feedback control is to provide operations conform to the ideal circuit shown in Fig. 5. Namely to:

1) Provide ac gain $V_{\mathrm{OUT}} = -G_0 \cdot V_{\mathrm{IN}}$.
2) Ensure dc operation point of $V_{\mathrm{OUT}} \approx V_{\mathrm{BIAS}}/2$.

Following section describes implementation of the linear controller with ramp-PWM modulator, allowing constant frequency operations of the switched-mode power stage.

A. Ramp-PWM Linear Controller

Small signal model of the control loop can be built around linearized power stage $V_{\mathrm{PWM}(s)}$ [15], as shown in Fig. 10.

The value of the duty-cycle $D(s)$ is obtained by superposition of V_{IN} and V_{OUT}

$$D(s) = -H(s)\left(G_1(s) V_{\mathrm{OUT}}(s) + G_2 V_{\mathrm{IN}}(s)\right) \tag{26}$$

where magnitude of V_{IN} is given by (10). Realization of the feedback control can be done with single operational amplifier controller [22], as shown in Fig. 11. Due to identical polarity of $G_1(s)$ and $G_2(s)$, signals from V_{OUT} and V_{IN} are connected

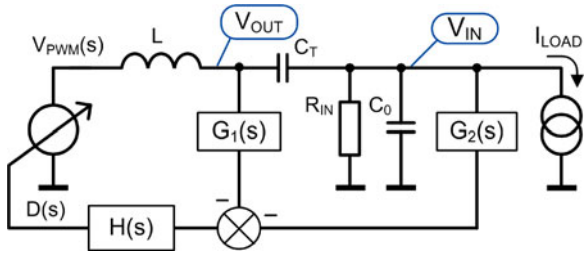

Fig. 10. Small signal model of the feedback control loop.

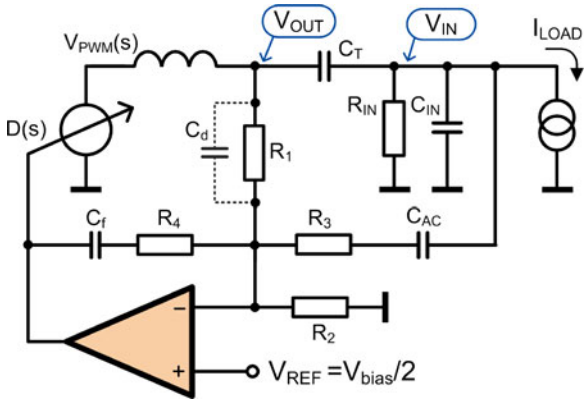

Fig. 11. Feedback control of Fig. 5 active capacitor. Resistors R_1, R_2 are used to set the dc operating point V_{OUT}, and R_1, R_3 ac gain G_0.

to inverting amplifier input. In this circuit, resistances R_1 and R_2 create voltage divider controlling the steady-state dc voltage V_{OUT}

$$V_{\mathrm{OUT(DC)}} = (1 + R_1/R_2)\, V_{\mathrm{REF}}. \tag{27}$$

Here, V_{REF} is to be set approximately to $V_{\mathrm{REF}} = 0.5 \cdot V_{DD(OpAmp)}$, e.g., also by a resistive divider. This allows to obtain steady-state dc voltage $V_{\mathrm{OUT(DC)}} \approx 0.5 \cdot V_{\mathrm{bias}}$.

It is to be noted, that R_2 is connected to the operational amplifier virtual zero. It follows that its value does not contribute to ac gain G_0. At low frequency (where impedance of C_f is negligible), ac gain G_0 is given as

$$G_0 = -\frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = -\frac{R_1}{R_3}. \tag{28}$$

Values of the feedback network C_f, R_4, C_d can be determined by using approaches of the control system engineering. In particular, C_f and R_4 are to be selected to ensure low gain at the switching frequency. In order to improve the regulation speed, high-frequency bypass capacitor C_d can also be added. The value of high-voltage coupling capacitor C_{AC} needs to be sufficiently high. This allows us to decrease the phase shift and attenuation of V_{IN} voltage at low frequency.

V. Implementation Example

Prototype of the switched-mode active capacitor was implemented on double-side PCB. Power stage was operated at $f_{\mathrm{SW}} = 40$ kHz. Simplified schematic of the active capacitor is

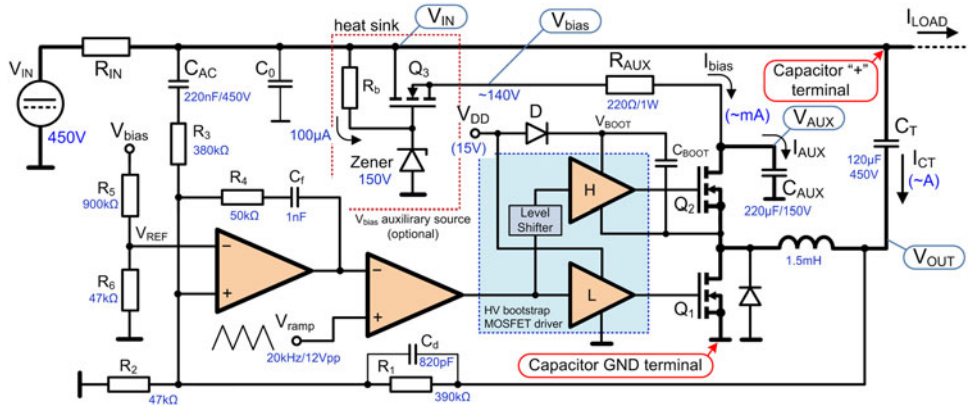

Fig. 12. Simplified schematic of the switched-mode high-voltage active decoupling capacitor.

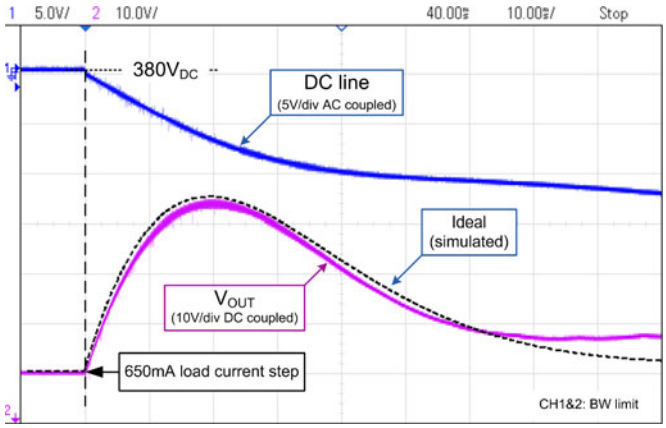

Fig. 13. 650 mA load current step applied to real dc supply with 10 Ω serial resistance, comparison with ideal (simulated) characteristic.

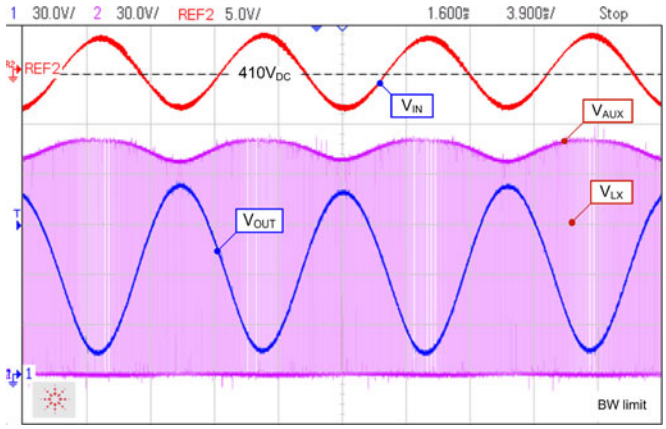

Fig. 14. DC decoupling circuit with power inverter (see Fig. 3, [11]). Parameters are summarized in caption Fig. 6. Power inverter deliver 1.5 kW power with 98% efficiency.

shown in Fig. 12. The power stage Q_1–Q_2 uses $V_{\rm DSS} = 150$ V 30-mΩ N-MOS transistors, and is controlled by a half-bridge bootstrap driver IC. The feedback loop controller and PWM comparator use ordinary JFET operational amplifiers. Circuit shown in Fig. 12 also contains optional voltage source $V_{\rm bias}$, implemented by source follower Q_3. In addition, a 150-V transient suppression diode was added to $V_{\rm LX}$ node. This diode allows us to reduce high voltage peak at the circuit's startup.

Measured waveforms of the active decoupling capacitor are shown in Figs. 13–15. Load step transient response shown in Fig. 13 allows us to demonstrate the ability of the circuit to compensate fast current fluctuations in the decoupled dc line. In measurement shown in Fig. 13, load current step of 650 mA was applied on 10 Ω resistor connected to real 380-V dc source ($R_{\rm IN} = 7\Omega, C_{\rm IN} = 7000$ μF/450 V). The nearly ideal load current step induces output voltage peak of +33 V. This voltage peak allows efficient attenuation of the load transient event.

Measured waveform obtained with the power inverter [11] in the configuration shown in Fig. 3 is shown in Fig. 14. Here, the power inverter was powered from $V_{\rm IN} = 450$ V dc source with 10 Ω internal resistance, and delivers 1.5 kW output power at 240 V ac output voltage. For this configuration, decoupling circuit allowed to bring the input voltage ripple below 10 $V_{\rm PP}$.

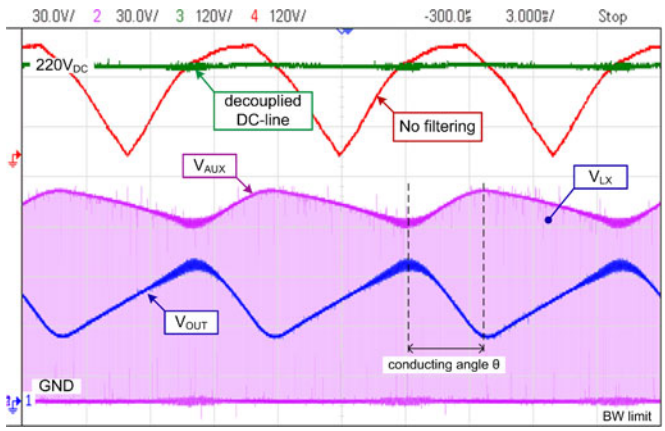

Fig. 15. Decoupling circuit filtering silicon-rectifier dc power source (produced by variable transformer). Comparison with nonfiltered full-wave rectified line voltage.

Transient response obtained by use the decoupling circuit with silicon rectifier is shown in Fig. 15. The dc load current 1.5 A results in generated filtering current $I_{CT(\rm RMS)} = 1.5$ A. In this configuration, the output voltage $V_{\rm OUT(peak-to-peak)}$

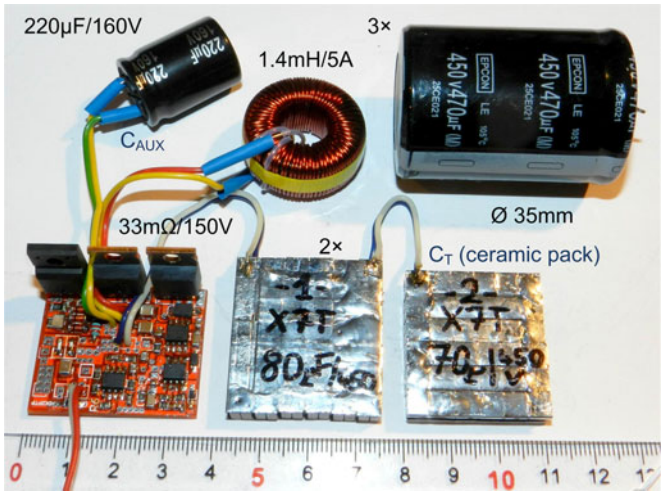

Fig. 16. Photography of 1300 uF active capacitor, comparison with 470 uF/450 V electrolytic capacitor. Only half of the total ceramic pack is shown in the figure.

reaches 40 V, which is lower than expected 56 V. This is caused by higher equivalent capacity of C_T at lower dc bias voltage (∼200 V), as pointed in Section III-b. It results, that due to the bias-dependent MLC capacitor C_T, the decoupling circuit presented in this paper exhibits nonlinear equivalent capacitance, when referred to the input dc-line voltage.

Realized active capacitor is shown in Fig. 16. The dominant space-demanding components are the 1.4 mH/5A sendust-core toroidal inductor, high-voltage MLCC capacitor C_T, and auxiliary capacitor C_{AUX}. The volume of the active electronic is negligible, thanks to the low-volume surface-mount design.

IV. Conclusion

This paper described circuit allowing us to decrease the volume of the high-voltage passive dc filters. The presented concept enables very-low volume implementation of the portable power electronics devices, suitable e.g., for mobile PV applications. Presented decoupling circuit contains shunt LC filter controlled by the low-voltage PWM electronics, allowing us to provide high power efficiency. The volume can be further reduced by providing single-IC (ASIC) circuit, including control part and bootstrap driver.

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