Three-level PWM Floating H-bridge Sinewave Power Inverter for High-voltage and High-efficiency Applications

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Abstract—This paper presents a topology of a single-phase floating full-bridge three-level PWM power inverter suitable for high-voltage/high-power DC-AC conversion. High power efficiency is obtained thanks to the slow (50/60Hz) biasing of the H-bridge power supply terminals, allowed by a particular arrangement and control of two complementary active neutral point clamped (ANPC) voltage source converters. As result, the main PWM switching voltage as well as the maximum drain-source voltage $V_{DSS}$ of related transistors are reduced to one-half of the input $V_{in}$ voltage. This is allowed by the internally generated and accurately balanced middle-node voltage $V_{rA}/2$. Consequently, advantageous $r_{DS(on)}$ of the low-voltage transistors, along with reduced switching PWM resistance, lower parasitic capacitances for given drain-source on-supply voltage. Generally, low $r_{DS(on)}$ voltage transistors considerably improves the overall power efficiency Application for high-voltage DC/AC power inverters. (ANPC full-bridge power inverter, non-isolated power inverter. Single-phase NCP power inverter.

I. INTRODUCTION

Generation of the multi-level PWM signal is a common technique allowing to reduce the triangular AC ripple currents and voltages in the switched-mode power converters, and namely in the power inverters [1-6]. Several multilevel architectures offer also reduction of the transistors’ drain-source voltage. This advantageously allows either to enlarge the choice of the switching devices (e.g. towards lower $r_{DS(on)}$), or to increase maximal power-supply voltage. Generally, low $V_{DSS}$ transistors present lower parasitic capacitances for given drain-source on-resistance $r_{DS(on)}$, compared to their high-voltage counterparts (section IV). Considering also reduced $Cf/f$ dynamic power, use of multilevel structure with low-voltage transistors considerably improves the overall power efficiency $\eta$ in whole output power range. Namely, lower input and output capacitances $C_{iss}$ and $C_{oss}$ of low-$V_{DSS}$ transistors, as well as reduced PWM switching voltage improve the low-power efficiency, whereas lower $r_{DS(on)}$ improves the high power conduction loss (depending on amount of serially connected transistors). Reduction of electromagnetic interferences (EMI) - thanks to lower $dV/dt$ is an additional advantage, regarding the current ElectroMagnetic Compliance standards. On the contrary, switched multi-level power converters require complex control algorithms often involving large analog/digital control circuits. Moreover, some topologies also contain extra passive components placed in the output current path, such as the diodes or capacitors. These passive components lead to a decrease of the power efficiency due to the unwanted voltage drop.

The generation of the multiple voltage level PWM voltage is based on the multilevel voltage source converter (VCS) power stages. The most frequently used VCS are listed e.g. in [6] and are shown in Fig. 1. We can mention namely:

a) Neutral point clamped VSC (diode or active clamped),

b) flying capacitors multilevel power stage,

c) cascaded H-bridge power stages.

These power stages can also be used in a full H-bridge topology, which is convenient for the multi-level power inverter design. The most commonly used VCS is the neutral point (or diode) clamped inverter NPC [5] Fig. 1 a), allowing to generate multiple voltage levels through the capacitors and diodes clamped to the middle point NP. This structure can be extended to any number of levels [7].

Fig. 1. Basic structures of multilevel half-bridge power stages [6]. a) neutral point (diode) clamped, b) flying capacitor and c) cascaded H-bridge power stages.
However, a precious neutral node balancing results in dominant three-level NPC configuration [8]. Flying capacitor structure Fig. 1 b) [9] offers attractive features when compared to the diode-clamped power-stage. Namely the clamping diodes are not present. Moreover, an extra switching state allows to regulate the flying capacitor voltage. Cascaded H-bridge topology Fig. 1 c) [10] consists in serially connected H-bridges, powered by the isolated DC voltage sources. Thanks to independent supply voltages, the voltage levels are easily scalable. On the contrary, the implementation of isolated DC voltage sources requires independent transformer windings or other floating power sources.

![Fig. 2. Three-level shifted-carrier PWM H-bridge structure [11] with related control signals.](image)

The phase shifted carrier PWM modulation [11] shown in Fig. 2 provides three-level PWM signal by generating asymmetrical duty-cycle for left and right half-bridges. Generated output voltage \( V_{\text{LX}(\text{OUT})} = V_{\text{LX(A)}} - V_{\text{LX(B)}} \) reaches three voltage levels: 0 and \( \pm V_{\text{DS}} \). This technique offers previously mentioned advantage of inductor current and output voltage ripple reduction. However, transistors regarding full drain-source voltage \( V_{\text{DSS}} > V_{\text{DD}} \) are required.

![Image](image)

Regarding the implementation of the medium and high-power multilevel MCS, the most frequently used structure is the neutral point clamped (NPC) power stage [5], [12], shown in Fig. 1 a) and detailed in Fig. 3 a). In a single-phase leg topology, the three voltage levels are obtained by the appropriate driving of the switches \( T_{1-4} \), and via clamping diodes \( D_1 \) and \( D_2 \). More in detail, the output voltage reach \( \pm V_{\text{DS}}/2 \) while \( T_1 \) and \( T_2 \) are simultaneously conducting, whereas \( -V_{\text{DS}}/2 \) is obtained by simultaneous conduction of \( T_3 \) and \( T_4 \). In these cases, the output power is delivered by the DC-link capacitors \( C_1 \) and \( C_2 \) (single phase variant). A zero voltage is obtained by simultaneous conduction of transistors \( T_2 \) and \( T_3 \). In this case, the output voltage is clamped to the low-impedance neutral point \( NP \) via one of the passive diodes \( D_1 \) or \( D_2 \).

While applying this modulation strategy to the sinewave PWM modulation (SPWM), it turns out that the central transistor \( T_2 \) remains conductive during entire positive half-period \( \Phi_0 \) of the output voltage \( V_{\text{OUT}} \), whereas gates of \( T_1 \) and \( T_3 \) are driven by fast complementary PWM signals. Likewise, generation of the negative half-period \( \Phi_1 \) of \( V_{\text{OUT}} \) is obtained by continuous conduction of \( T_3 \), and complementary PWM modulation of \( T_2 \) and \( T_4 \) transistors gates.

It results, that important portion of the output current is delivered by passive components \( D_1 \), \( D_2 \) and by DC-link capacitor \( C_1 \) and \( C_2 \) (single phase variant). Above the neutral point (NP) balancing, the power losses occurring in the capacitors and diodes yield a conversion efficiency loss. Ref. [13] introduces an active-NPC, where the clamping diodes are substituted by active switches \( T_{\text{AUX1}} \) and \( T_{\text{AUX2}} \). This result in the important efficiency increase [14]. Thanks to the clamping diodes (switches), both (A)NPC structures from Fig. 3 reduce stress on the transistors \( V_{\text{DSS}} \). A single-phase full-bridge configuration of NPC VCS from Fig. 3a) allows to obtain a five-level output voltage [15]. However, capacitor power losses and capacitor balancing remain a design issue of the both full-bridge and three- phases power inverters [16], [17], [18].

![Fig. 3. Detail of the neutral-point clamped a) and active neutral-point clamped VCS [13] allowing eliminate the power losses in the clamping diodes \( D_1 \) and \( D_2 \).](image)

In the following text, structure of the three levels PWM full-bridge power inverter allowing to reduce maximal \( V_{\text{DSS}} \), reduce output ripple current, and provide automatic balancing of the middle-point voltage is described. Topology is derived from single phase ANPC VCS, whereas the switches control sequence has been modified. The structural description of the power inverter is presented in section II. Section III describes in detail the implementation and feedback control scheme. Section IV discusses the choice of power transistors, whereas the physical implementation and measured results of 450V_Dc input and 230V_AC output voltage 2kW power inverter are shown in section V.
II. THREE-LEVEL PWM FLOATING H-BRIDGE TOPOLOGY

Architecture of the three-level PWM sinewave power inverter presented in this paper is based on two floating dual-NMOS half-bridges operating with PWM modulation at switching frequency $F_{SW}$. The structure uses a virtual middle-point voltage $V_{MID} = V_{DD}/2$. This node voltage is generated by the high-impedance (low-consumption) voltage divider. In the presence of phase signal $\Phi (50/60Hz)$, $V_{MID}$ becomes a low-impedance node and is accurately balanced to $V_{DD}/2$. As shown in following, $V_{MID}$ voltage node delivers zero output current $I_{MID} = 0$, which allows its compact and low power realization. Presented structure allows to use transistors with half-$V_{DD}$ maximum drain-source voltage $V_{DSS}$. Thanks to a reduced drain depletion region, these transistors present lower parasitic capacitance and on-resistance. As consequence, the dissipated heat is very low, which enables very low-volume realization, suitable e.g. for portable/mobile PV (photovoltaic) applications.

A. Architecture of the Power Inverter

Architecture of the three-level PWM power inverter is shown in Fig. 4. In this figure, we notice:

a) voltage divider creating the high-impedance node $V_{MID} = V_{DD}/2$,

b) two floating half-bridge power stages with small (few µF) coupling capacitors $C_B$,

c) supply voltage synchronous switches $SW_{A\_H,H,L}$, $SW_{B\_H,H,L}$ switching at low (output sinewave) frequency $f(\Phi) = 50/60Hz$.

Operation of the floating H-bridge topology can be separated in two states, depending on the output sinewave polarity $\Phi$. During the first half-period ($\Phi = H$), the left half-bridge (A) is powered from $V_{DD}$ and $V_{MID}$, whereas the right half-bridge (B) is powered from $V_{MID}$ and GND. In other words, $A_{H} = V_{DD}$, $A_{L} = B_{H} = V_{MID}$ and $B_{L} = GND$.

During the second half-period ($\Phi = L$), the half-bridge supply voltages are inverted. It means, that $\Phi = H$ results in $V_{LX(A)}$ switching between $V_{DD}$ and $V_{MID}$, whereas $V_{LX(B)}$ between $V_{MID}$ and GND. On this account, output voltage $V_{LX(A)} - V_{LX(B)}$ is divided by two compared to the traditional H-bridge topology, whereas all power transistors (half-bridges and switches SW) operate with reduced drain-source voltage $V_{DD}/2$. In comparison with the NPC inverter structures [15], [16], transistors in Fig. 4 connected to the output nodes ($V_{LX(A),B}$) are fast-switching devices, whereas switches connected to the DC-link $V_{DD}$, $V_{MID}$ and GND voltages are the slow-switching devices.

Idealized switched-mode simulation of the DC/AC inverter from Fig. 4 is shown in Fig. 5. Here, we can see that during the first half-period $\Phi = H$, the output voltage $V_{LX(A)} - V_{LX(B)}$ is divided by two compared to the traditional H-bridge topology, whereas all power transistors (half-bridges and switches SW) operate with reduced drain-source voltage $V_{DD}/2$. Thanks to a reduced drain depletion region, these transistors present lower parasitic capacitance and on-resistance. As consequence, the dissipated heat is very low, which enables very low-volume realization, suitable e.g. for portable/mobile PV (photovoltaic) applications.
Detailed Operations
This section describes operations of the floating H-bridge topology shown in Fig. 4. The operation is described in four phases $Φ_{\text{A-D}}$, depending on the PWM signal level and polarity $Φ$ of the output generated voltage $V_{\text{OUT}}$. These operations are depicted in following figures Fig. 6 a-d).

In the first phase $Φ_{\text{A}}$, left half-bridge is powered from $V_{\text{DD}}$ and $V_{\text{MID}}$, whereas right half-bridge from $V_{\text{MID}}$ and GND (situation from Fig. 4). The dashed line corresponds to the output current flow. This current passes through $SW_{\text{A1}}$, $Q_{\text{AH}}$ and load to $Q_{\text{BH}}$ and $SW_{\text{B4}}$. During this conduction phase, the inductor current linearly increases, whereas the voltage $V_{\text{MID}}$ remains in the steady-state thanks to charged capacitors $C_{\text{IN}}$ and $C_{\text{BH}}$. During the second phase ($Φ_{\text{B}}$), the polarity of PWM signal is inverted. The decreasing inductor current circulates through $SW_{\text{A3}}$, $Q_{\text{AL}}$ and load to $Q_{\text{BL}}$ and $SW_{\text{B3}}$. In this case, the current forms a closed loop, which means, that there is ideally no current flowing into the middle-point node $V_{\text{MID}}$.

The operations of 3$\text{rd}$ and 4$\text{th}$ phases $Φ_{\text{C}}$ and $Φ_{\text{D}}$ are similar, except that the left half-bridge is powered from $V_{\text{MID}}$ and GND, whereas right half-bridge from $V_{\text{DD}}$ and $V_{\text{MID}}$. This can be also seen from the idealized simulation previously shown in Fig. 5.

During the switching between phases $Φ = \text{H}$ and $Φ = \text{L}$, small (few $\mu$F) capacitors $C_{\text{B}}$ are connected alternately to the upper and lower voltage-divider capacitors $C_{\text{IN}}$. This signifies that any DC difference between $(V_{\text{DD}}-V_{\text{MID}})$ and $(V_{\text{MID}}-\text{GND})$ is cancelled by the continuous charge transfer between upper and lower capacitors $C_{\text{IN}}$. While considering the frequency of generated sinewave $f_{\text{OUT}}$, the cancellation of this error is provided 2Φ-times per second. In other words, for frequencies below $f_{\text{OUT}}$, the impedance seen in the node $V_{\text{MID}}$ is:

$$Z_{\text{MID}} = \frac{1}{2}(R_{\text{IN}}/\|Z(C_{\text{IN}})/\|Z(2C_{\text{B}}f_{\text{OUT}}))$$  \hspace{1cm} (1)

The fact that the MID-node impedance is dominated by capacitors $C_{\text{IN}}$ and $C_{\text{BH}}$, allows to reduce the DC bias current $I_{\text{bias}}$, through $R_{\text{IN}}$ to fraction of mA. Resistances $R_{\text{IN}}$, then only ensure the correct biasing of $C_{\text{IN}}$ in the absence of clock signal $Φ$ (i.e. when power-inverter is turned off).

III. POWER INVERTER CIRCUIT IMPLEMENTATION

Except twelve power transistors (eight for the low-frequency switches $SW$ and four for the floating H-bridge), the implementation example shown here uses ordinary industrial ICs such as the high-voltage bootstrap MOSFET drivers, basic logical cells, and operational amplifiers. Following paragraphs describe the implementation of a) low-frequency switches $SW$, b) floating H-bridge and c) example of the feedback control loop.

![Fig. 6. Four operating phases $Φ_{\text{A-D}}$ with highlighted $I_{\text{bias}} = 0$ and output current paths. For simplicity, only one inductor is shown in the figures.](image-url)
A. Low Frequency Power-Supply Switches SW

As shown in Fig. 4 and Fig. 6, the power inverter contains two pairs of power supply switches, powering nodes A\_L(LLL) and B\_L(LLL) of the floating half-bridges. These switches operate at low frequency (50/60Hz) and exhibits therefore nearly zero dynamic switching losses compared to H-bridge transistors (section III.B). On this account, a very-low $r_{DS(on)}$ and potentially highly capacitive power transistors can be used advantageously. Circuit of the left-side power-supply switch is shown in Fig. 7. Right power-supply switch is identical except the inverted driving signal $\Phi$. (see Fig. 4).

![Fig. 7. Left side power-supply switch with HV bootstrap drivers DRV\_AB, level shifter DRV\_C, and V\_MID+V\_CC voltage generator. Right power-supply switch is identical except the inverted driving signal $\Phi$.](image)

The main target in the power-supply switch design is the accurate triggering of the output signals $A\_H$ and $A\_L$. In fact, transitions of these signals should be perfectly synchronous. If this is not the case, floating H-bridge transistors and capacitors $C\_H$ operate shortly under full $V\_DD$. This results in potential transistor damage or high EMI due to high current spikes in capacitors $C\_H$.

In order to provide synchronization of $A\_H$ and $A\_L$ power nodes, solution shown in Fig. 7 is based on the input driver/level-shifter DRV\_C. This driver contains one ground-referred channel (L), and one floating channel (H) driven by a pulsed latch level shifter [19],[20]. Implementation of this level shifter is based on the industrial MOSFET driver [21]. This IC allows to obtain approximately 10ns propagation delay mismatch and offers very low consumption and implementation volume.

In order to enable operation of the high-side bootstrap driver DRV\_B, voltage $V\_MID + V\_CC$ should be created. This voltage is obtained by rectification of the low-side bootstrap voltage $V\_BOOT$. Rectification and filtering of $V\_BOOT$ is provided by means of silicon diode $D\_2$ and tantalum capacitor $C\_H$. The capacitor $C\_H$ is charged by $C\_BOOT(a)$ when $A\_L = V\_MID$ and $V\_BOOT = V\_MID + V\_CC$. On this account, value of $C\_BOOT(a)$ should be large enough (>10µF), in order to provide sufficient charge transfer towards $C\_H$. Moreover, nodes $V\_MID + V\_CC$ of the left-side and right-side power-supply switches are connected. This results in double (100/120Hz) charging rate of $C\_H$.

Implementation shown in Fig. 7 enables to produce sufficient gate-driving voltage of $SW\_L$ of $V\_DD + V\_CC$, reduced by three forward diode drops of $D\_1$, $D\_1$, and $D\_3$. Bootstrap drivers DRV\_A and DRV\_B are standard single-input IC bootstrap drivers with embedded 500ns dead-time generator.

B. Floating H-Bridge Control

Fig. 4 and Fig. 6 show that the supply voltages of the left and right half-bridges are switched alternately between GND–$V\_MID$ and $V\_MID$–$V\_DD$ voltage domains. This requires particular handling of $Q\_H$ and $Q\_L$ transistor gate voltages. For this purpose, floating capacitor $C\_F$ (~47µF (Fig. 8) charged to $V\_CC$ ensures the powering of the bootstrap driver DRV\_E during the floating-mode operations. When $A\_L = GND$, capacitor $C\_F$ is charged to $V\_CC$ (~15V) via $D\_4$ and the bootstrap driver DRV\_E operates in GND–$V\_CC$ voltage domain. When $A\_L = V\_MID$ and $A\_H = V\_DD$, capacitor $C\_F$ remains charged to $V\_CC$, ensuring the powering of the bootstrap driver DRV\_E during whole half-period $\Phi$. Driver DRV\_E then operates in $V\_MID$–$(V\_MID+V\_CC)$ voltage domain.

In the circuit of floating H-bridge shown in Fig. 8, the input PWM signal is level-shifted by means of pulsed latch level shifter integrated in DRV\_D. Similarly to the solution shown in Fig. 7, the level shifter is realized by IC driver [21], allowing to provide low-volume and cost-effective integration.

![Fig. 8. Left floating half-bridge with input level shifter integrated in DRV\_D and bootstrap driver DRV\_E. The power supply of DRV\_E is ensured by the floating capacitor $C\_F$ and diode $D\_4$. Right half-bridge producing $V\_LOAD$ is identical except the inverted driving signal PWM.](image)

The power-off (standby) regime of the inverter is achieved by setting the transistor $Q\_H$, $Q\_L$ of Fig. 8 half-bridges to high impedance. This is obtained by two low power-high-voltage

![Fig. 9. Standby mode control of Fig. 8 bootstrap driver DRV\_E.](image)
voltage transistors, pulling down the shutdown pins of drivers DRV E to GND via a high-value coupling resistances (Fig. 9). During the standby regime, the switches SW (Fig. 7) are preferably active, in order to ensure the balancing of the node $V_{\text{MID}}$ (power consumption in standby regime was $\approx 2\text{mA}$ at 450V).

C. Feedback Control Loop

In order to provide high spectral purity of $V_{\text{OUT}}$, a feedback control loop of the power inverter output voltage was implemented. The control of the power inverter is basically identical to the control approaches developed for the bridge tied load (BTL) class-D audio amplifiers. Here, the quality of amplifier is directly related to the quality and speed of the regulation loop. As example, linear controller with ramp-PWM modulator is presented in [22]. Ref. [23] presents example of a nonlinear sliding-mode controller with hysteretic comparator. Compared to these concepts, implementation of the multilevel-PWM power stages usually requires complex modulation scheme as the multilevel shifted carriers PWM modulation [11].

Structure of the power inverter presented in this paper requires generation of single PWM control signal, whereas left and right half-bridges are controlled by complementary inputs PWM and PWM. In order to realize appropriate controller transfer function, output voltage $V_{\text{OUT}(A)} - V_{\text{OUT}(B)}$ is transferred to the low-voltage single-ended domain GND - $V_{\text{CC}}$:

$$V_{\text{OUT LOW}} = \frac{V_{\text{CC}}}{2} + G_{b}(V_{\text{OUT}(A)} - V_{\text{OUT}(B)})$$  \hspace{1cm} (2)

A linear controller can be implemented e.g. by standard single-OpAmp PID controller [24], ramp-signal generator and a comparator. This controller is shown in Fig. 10.

![Fig. 10. Linear PID controller [24] with ramp (triangle) PWM modulator for Fig. 4 floating H-bridge sine wave inverter.](image)

Design of the controller transfer function can use any feedback-loop optimization method of the DC/DC converters such as [25] or [26]. However, a crossover distortion occurring during the phase transitions $\Phi$ can induce oscillations in the output voltage. These oscillations create dangerous voltage and current peaks, as well as undesired electromagnetic interferences. In the power inverter described here, the parasitic crossover oscillations are accentuated by required fast duty-cycle transitions from 0% to 100% and vice versa. As shown in example Fig. 11, the output voltage is required $V_{\text{OUT(B)}} = V_{\text{MID}}$ in the time of transitions. When considering e.g. transition $\Phi \rightarrow \bar{\Phi}$, the duty-cycle steps instantaneously from 0% $\rightarrow$ 100%. On this account, $V_{\text{ERROR}}$ should contain very fast 0 $\rightarrow V_{\text{CC}}$ and $V_{\text{CC}} \rightarrow 0$ edges.

![Fig. 11. Low-voltage measured example of $V_{\text{ERROR}}$ for single-level ramp modulator. The transition of $V_{\text{ERROR}}$ creates oscillation in the output voltage during the phase transitions.](image)

A smooth transition of $V_{\text{ERROR}}$ can be obtained by applying two-level triangle-wave signal to the PWM comparator from Fig. 10. This signal can be created by e.g. two OpAmp generator shown in Fig. 12. Here, the DC level of the triangle wave is modulated with polarity signal $\Phi$ (signal $\Phi$ modulates the threshold voltage of the hysteretic comparator OA1). Moreover an extra capacitor coupled to $\Phi$ was added, allowing to accelerate the rising/falling edges of the output voltage $V_{\text{RAMP}}$ during the polarity transitions.

Example of the signal generated by circuit from Fig. 12 is shown in Fig. 13. Here, signal $V_{\text{ERROR}}$ is equal to $V_{\text{CC}/2}$ at the time of transitions. As result, both $V_{\text{ERROR}}$ and $V_{\text{OUT}}$ exhibit smooth polarity transitions. This can be seen on the voltages captured in Fig. 13, and also on the output voltage waveforms shown in section V.

![Fig. 12. Two-level triangle wave signal generator. Signal “sync $\Phi$” is used to synchronize the transition $\Phi$ with ramp signal.](image)

It is to be noted that the analog control scheme also requires synchronization of phase transition $\Phi$ and ramp signal $V_{\text{RAMP}}$ (note: this is natural when digital control is used and $f_{\text{RAMP}} = \pi f(\Phi)$). This has been done by enabling the phase transition $\Phi$ with the rising edge of signal “sync $\Phi$” shown in Fig. 12 and highlighted in Fig. 13.
As mentioned in section II, power inverter shown in Fig. 4 allows to use transistors with low breakdown voltage $V_{DSS}$ close to $V_{DD}/2$. One already mentioned feature of the presented structure is the slow switching frequency (50/60Hz) of power-supply switch transistors shown in section III. A. On this account, efficiency optimization of this part aims only to reach the lowest possible drain-source on-resistance $r_{DS(on)}$. Indeed, a slow 50/60Hz switching rate renders the dynamic losses of any highly-capacitive transistors negligible, compared to the switching power dissipated in the floating H-bridge.

On the contrary, transistors used in the floating H-bridge exhibit both static and dynamic power losses. Generally, transistors designed for lower $V_{DSS}$ close to $V_{DD}/2$ exhibit several-times better $r_{DS(on)}\times Q$ (charge) factor of merit (FOM). This assumption results from silicon limit rule for planar MOSFETs [27]:

$$r_{DS(on)}\times Area = \frac{4}{e\cdot\mu_s\cdot E_C}BV^{2.5}\left(\Omega\cdot cm^2\right)$$  \hspace{1cm} (3)

where $E_C$ is the critical electric field and $BV$ the transistor breakdown voltage referring to the breakdown voltage of the PN junction. In planar MOSFET structure, this junction (drift region) provides high forward blocking capability by the extension of a depletion layer on both PN junction sides. Reduction of the junction size allowed by the reduction of $V_{DSS}$ yields a high ($BV^{2.5}$) decrease of the parasitic capacitances and on-resistance of the transistor.

Advantageously, $r_{DS(on)}\times Q$ FOM can be improved above the Si limitation (3) by employing advanced transistor topologies. As example, recent hexagon trench MOSFET, or Super-Junction transistors [28] (used in the final prototype) reach lower $r_{DS(on)}\times Area$ FOM and lower power coefficient (~1.5) than theoretical planar Si-limit rule. Similarly, the power efficiency or inverter maximal operating voltage $V_{DD(max)}$ can be increased by using recent wide-bandgap semiconductors such as GaN or Silicon Carbide (SiC) devices [29].

Although Eq. (3) shows that the basic figures of merit are degraded for high voltage devices, an exact rule cannot be established due to the different geometries for low and high voltage devices. An representative set of parameters for low and high $V_{DSS}$ devices from three fabricant (presenting lowers $r_{DS(on)}$ for given $V_{DSS}$ in TO-220) are shown in Tab. 1. Here, except the STxx transistors, degradation of the parameters can be observed.

### Table I.

<table>
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<tr>
<th>Reference</th>
<th>$V_{DSS}$ (V)</th>
<th>$r_{DS(on)}$ (mΩ)</th>
<th>$Q_s$ (nC)</th>
<th>$Q_d$ (nC)</th>
<th>$C_m$ (pF)</th>
<th>$C_{oss}$ (pF)</th>
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### Table II.

<table>
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<tr>
<th>Parameter</th>
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<tbody>
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<td>$V_{DD}$ operating range</td>
<td>390 - 450V</td>
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<td>Max. output power</td>
<td>2000W</td>
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<tr>
<td>Static $V_{DD}$ power consumption</td>
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<td>Switching frequency</td>
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<td>THD+N</td>
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<tr>
<td>Peak Efficiency</td>
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<tr>
<td>15V $V_{CC}$ quiescent current</td>
<td>60mA</td>
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<td>Power MOSFETs</td>
<td>SuperJunction Si: 17mΩ/250V</td>
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<tr>
<td>Power Inductors</td>
<td>1.4mH/7A toroid softschott core</td>
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<tr>
<td>Device volume (cm³)</td>
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<tr>
<td>Power density (W/cm³)</td>
<td>11W/cm³</td>
</tr>
</tbody>
</table>

1 $V_{DD} = 240V_{MAX}$
2 $P_{DC} = 0$
3 $P_{DC} = 1kW$
4 consumption of analog control electronic and MOSFET drivers

### V. REALIZATION AND MEASUREMENT RESULTS

Prototype of the power inverter was realized on double-side PCB with 70µm Cu layer, allowing to handle high (12A peak) output current. Maximal supply voltage $V_{DD(max)} = 450V$ and maximal output power $P_{OUT(max)} = 2kW$ correspond to the maximum rating of used transistors, capacitors, and power inductors. Main parameters obtained with realized sample of the power inverter are summarized in following Tab. 2.
A. Output Voltage

Captures of the output voltage waveforms were provided for output powers \( P_{\text{OUT}} = 0 \)W and \( P_{\text{OUT}} = 2000\)W. For the sake of clarity, capture \( P_{\text{OUT}} = 0 \) shown in Fig. 14 contains left-side signals only. In this figure, the accurate balancing of the node \( V_{\text{MID}} = V_{\text{DD}}/2 \) can be observed.

The full load operation \( P_{\text{OUT}} = 2\)kW is shown in Fig. 15. Here, filtering of the input voltage \( V_{\text{DD}} \) was decreased (17Ω / 470µF RC filter inserted in serie to 450V DC voltage source). The decreased filtering of the input voltage allows to demonstrate high immunity against the input \( V_{\text{DD}} \) voltage ripple. This is important namely with regard to the floating bootstrap drivers, powered by the capacitors \( C_0 \) and \( C_1 \). In Fig. 15, an AC coupling of the \( V_{\text{MID}} \) and \( V_{\text{DD}} \) voltages within switching period \( \Phi \) can be observed. It results, that both voltages \( V_{\text{OUT}(A)} \) and \( V_{\text{OUT}(B)} \) contains 100Hz compound of the \( V_{\text{MID}} \) voltage ripple. However, by using the differential sensing (2), the the middle-node 100Hz AC component is removed from regulated voltage \( V_{\text{OUT}} = V_{\text{OUT}(A)} - V_{\text{OUT}(B)} \) shown in Fig. 15.

B. Power Efficiency

Power efficiency was measured at \( F_{\text{SW}} = 35\)kHz and \( V_{\text{IN}} = 450\)V voltage source with \( R_{\text{IN}} = 17\)Ω input impedance. The input voltage decoupling was realized by 470µF/450V electrolytic capacitor and the converter was operating under steady-stage condition. The impedance of input RC filter causes the \( V_{\text{DD}} \) voltage decrease with increasing output power (see Fig. 15). Resulting power efficiency is shown in Fig. 16 and exhibits relatively stable behavior in the middle and low-power area. The peak efficiency 98.6% is at 800W output power and its position can be adjusted by the switching frequency \( F_{\text{SW}} \). The measured power efficiency includes also the power delivered by \( V_{\text{CC}} \) voltage to the bootstrap drivers and control circuits.

C. Startup Inrush Current Limitation

Entire power inverter control and driving circuit is powered from the switched-mode 75kHz DC/DC converter providing output voltage \( V_{\text{CC}} = 15\)V. The startup sequence requires this voltage to be present before powering the main \( V_{\text{DD}} \) node voltage. This allows to set all bootstrap drivers outputs in low impedance, preventing the power transistor from an eventual damage during the rising of theirs \( V_{\text{DS}} \) voltages. Solution employed in the prototype allowing to prevent the inverter from an eventual damage is shown in Fig. 17. Here, the low-consumption 5A relay switches on the inverter \( V_{\text{DD}} \) with embedded delay of \( \approx 5\)s. This delay is realized by RC filter connected to 15V \( V_{\text{CC}} \) voltage. In other word, the relay can be switched-on only after the detection of the \( V_{\text{CC}} \) voltage, and switch off immediately after \( V_{\text{CC}} \) voltage disappears (thanks to the schottky diode \( D_A \)).

Fig. 14. Output waveforms capture for \( V_{\text{DD}} = 450\)V and \( V_{\text{OUT}} = 230\)VAC RMS. Switching frequency was 35kHz and output voltage frequency 50Hz.

Fig. 15. Measurements of \( V_{\text{L(A)}}, V_{\text{OUT(A)}}, \) and \( V_{\text{OUT}} = V_{\text{OUT(B)}}, V_{\text{OUT}(A)} \) for \( P_{\text{OUT}} = 2000\)W (math channel \( V_{\text{OUT}} \) scale is 100V/div). The \( V_{\text{DD}} \) filtering was voluntarily decreased (17Ω/470µF) in order to demonstrate the noise immunity of the power inverter (\( V_{\text{OUT}(A)} = 330\)V \( V_{\text{OUT}(B)} = 230\)V).
In the startup circuit, an extra 2kΩ/2W resistor was added across the contact, allowing a slow charging of the input 450V decoupling capacitor. This realizes limitation of the power inverter input inrush current. Moreover, this resistor and diode Ds also enables to achieve low DC voltage across the contact (during the switch-on/off), allowing to protect the relay switching arm from an electric arc damage.

D. PCB Implementation of the Power Inverter

Realization of the power inverter is shown in Fig. 18, and configuration including toroidal inductors before the final assembly in Fig. 19. The implementation contains set of eight power transistors of the supply-voltage switches SW, and four for the floating H-bridge.

The supply-voltage switch transistors exhibit low dissipated heat and require only reasonable small heat sink (not shown in Figs. 18 and 19). The H-bridge fast-switching transistors exhibit higher power dissipation and are spaced by 2cm gap. This gap enables better distribution of the heat. However, thanks to very high power efficiency, the outside temperature of the power inverter does not exceed 60°C at 2kW output power. The large electrolytic capacitors CIN (68µF/250V) are bypassed by the high-voltage low-ESR 2.2µF/250V multilayer ceramic capacitors. Similarly, coupling capacitors CB (22µF/250V, not shown in Figs. 18 and 19) are bypassed by the low-ESR ceramic capacitors.

All gate drivers also contain output 15Ω resistors allowing to limit the VLL output rising/falling slopes, and reducing thus the high frequency oscillations on the transistors terminals.

CONCLUSION

Presented paper describes the topology of the high power-efficiency DC–AC inverter. It was shown, that the slow DC-biasing of the H-bridge supply terminals allows to reduce the PWM switching voltage. Reduced dynamic losses CFI, together with better parameters of the low voltage transistors allowed to decrease the total dissipated power in whole output power range. This is suitable namely for ultra-compact portable applications, where the low device volume is limited by the high required heat transfer. Alternatively, advantageous VDI/2 biasing of all power transistors allows to use the power inverter up to very high voltage, which is enabled by the recently available high-voltage Silicon-Carbide (SiC) power transistors.

REFERENCES


[21] see product datasheet a) IRS2186 (www.irf.com) or b) NPC5181 (www.onsemi.com).


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