Design of CMOS analog integrated circuits as readout electronics for high-T_C superconductor and semiconductor terahertz bolometric sensors

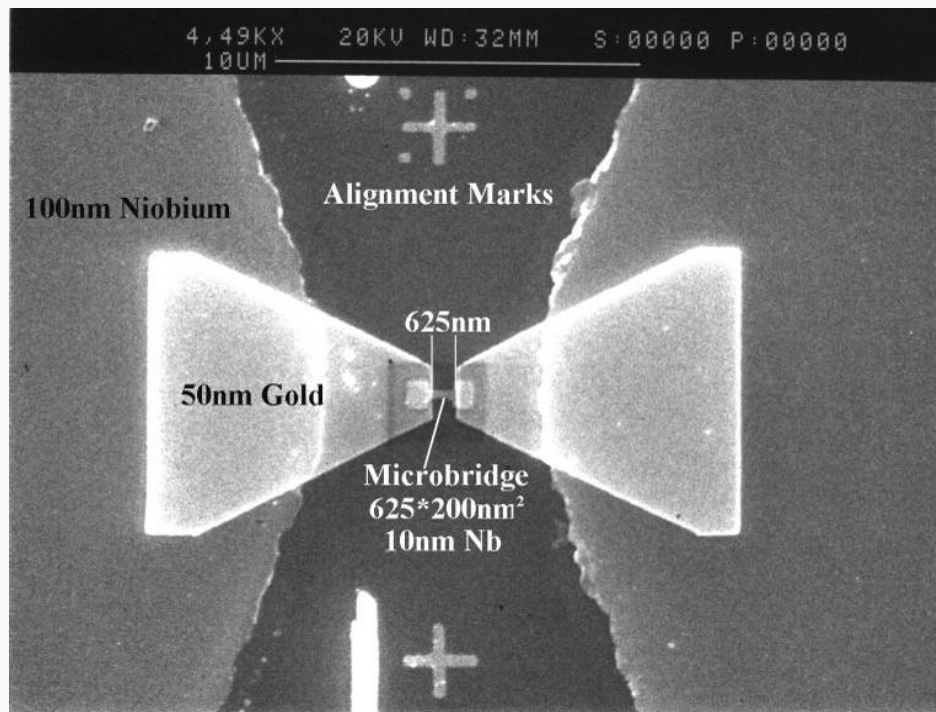## Vratislav Michal

Supervisors:

Prof. Alain Kreisler, Laboratoire de Génie Electrique de Paris-Supélec, UPMC-P6

Assoc. Prof. Jiří Sedláček, DTEEE - Brno University of Technology
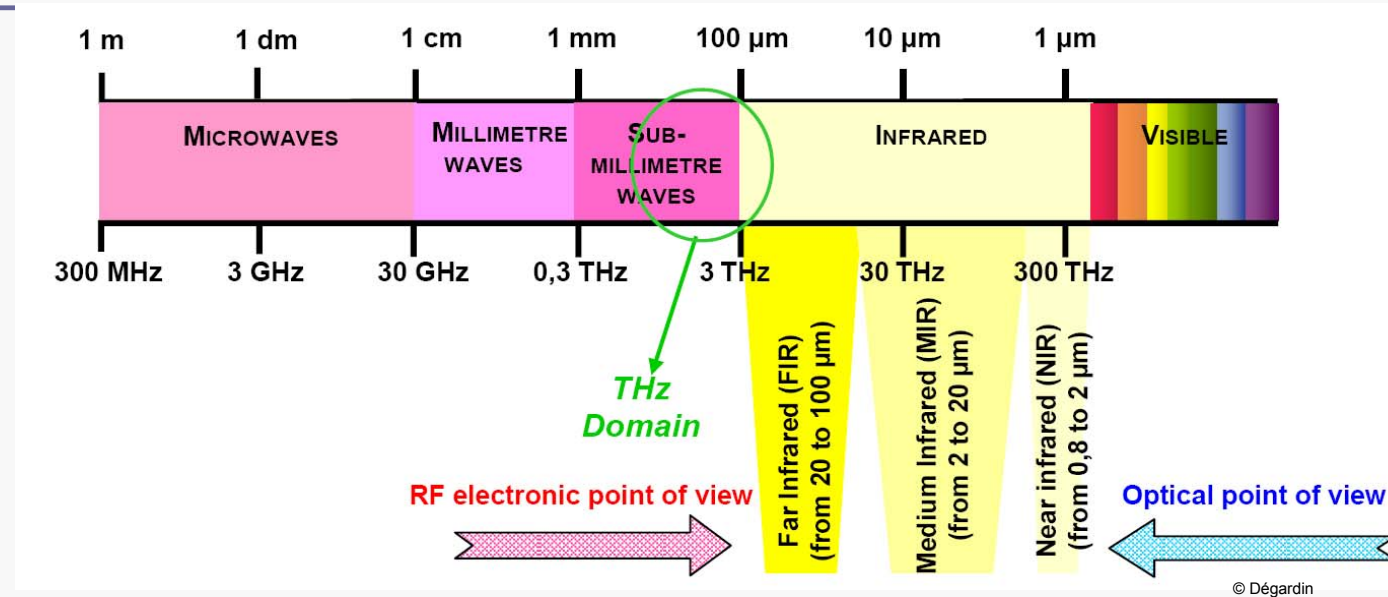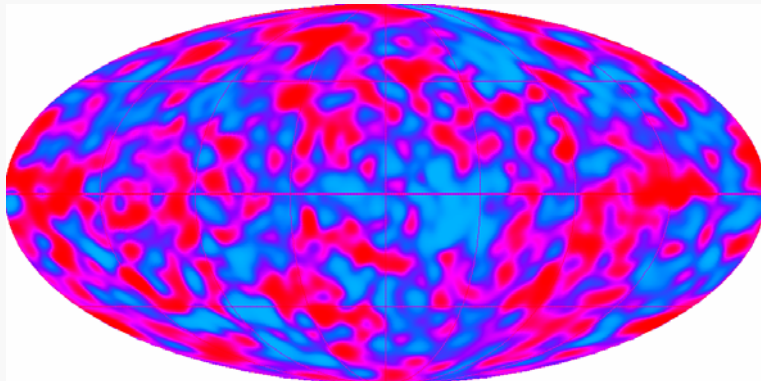
Gif, June 10th 2009
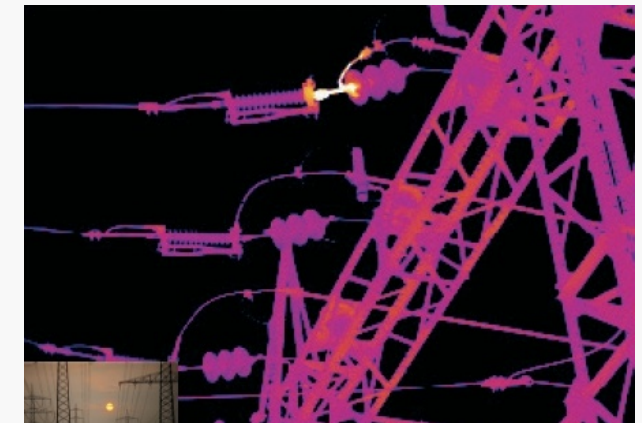
I.
Introduction

THz detection and imaging

Research applications

Cosmic Microwave background exploring
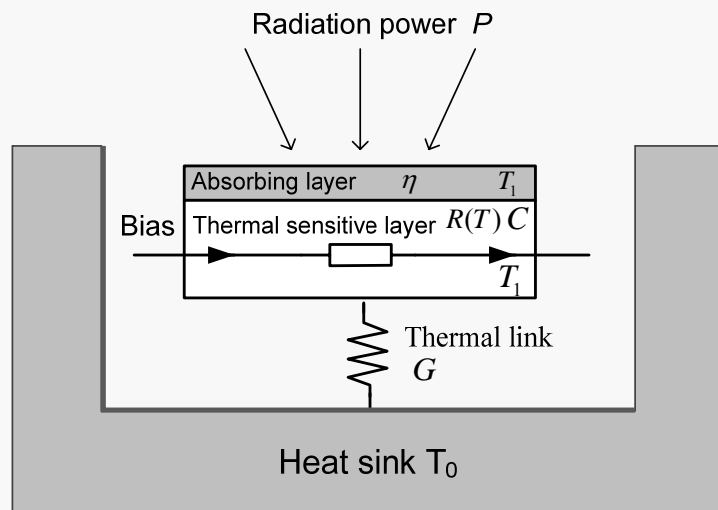
[COBE-Nobel prize in physics 2006]

Civil applications
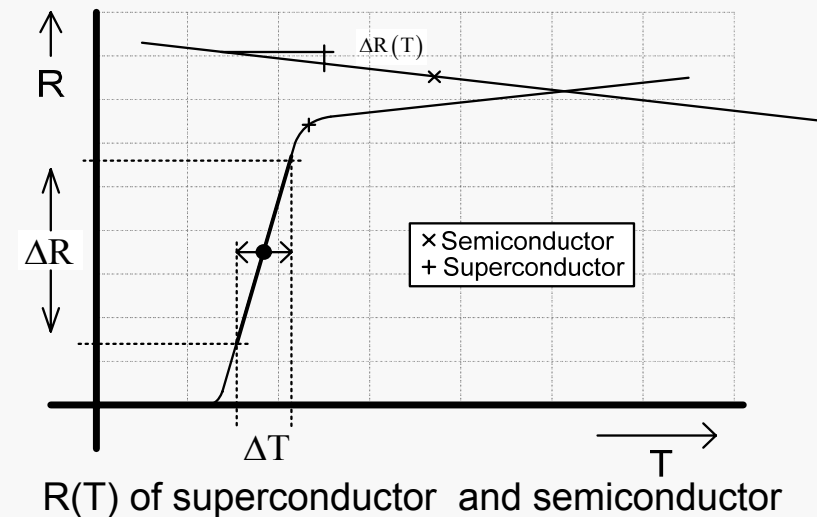
High voltage insulator under discharge

[ulis-ir website]

Other fields of applications:

Spectroscopy

Civil security, medical
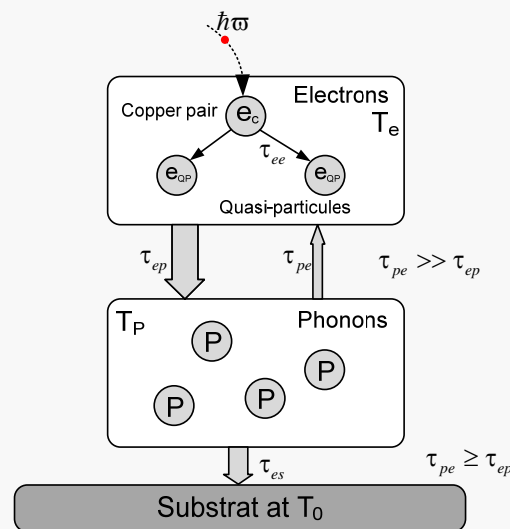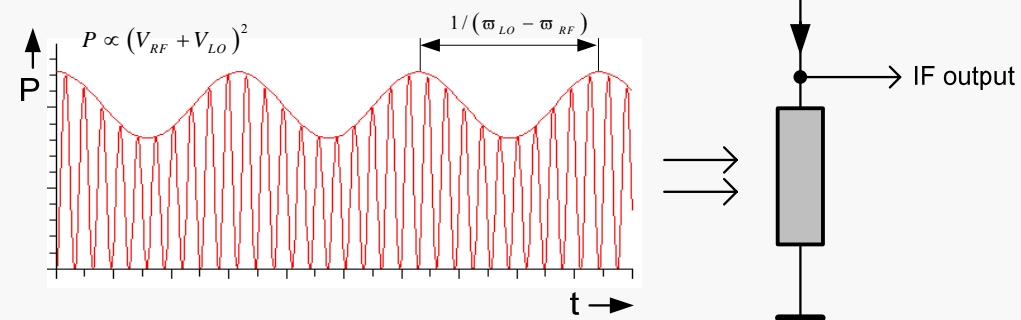
Military application etc…

(THz) Bolometric detectors

Radiation power P

Absorbing layer η T_1

Bias   Thermal sensitive layer $R(T)$ C

T_1

Thermal link G

Heat sink T_0

R(T)

R

$\Delta R(T)$

ΔR

× Semiconductor
+ Superconductor

ΔT

T

R(T) of superconductor and semiconductor

[subject of other Nanotime theses]

Heterodyne detection:

$\hbar\varpi$

Copper pair e_c Electrons T_e

τ_{ee}

e_{QP} e_{QP}

Quasi-particules

τ_{ep} τ_{pe} $\tau_{pe} \gg \tau_{ep}$

T_P Phonons

P   P   P   P

τ_{es} $\tau_{pe} \geq \tau_{ep}$

Substrat at T_0

Superconducting Hot Electron
Bolometer (HEB)

$P \propto (V_{RF} + V_{LO})^2$

$1/(\varpi_{LO} - \varpi_{RF})$

P

t

DC bias

IF output

Characterization of new generation THz detectors: A CRUCIAL ROLE OF ELECTRONICS

blocks developed in the frame of the PhD thesis
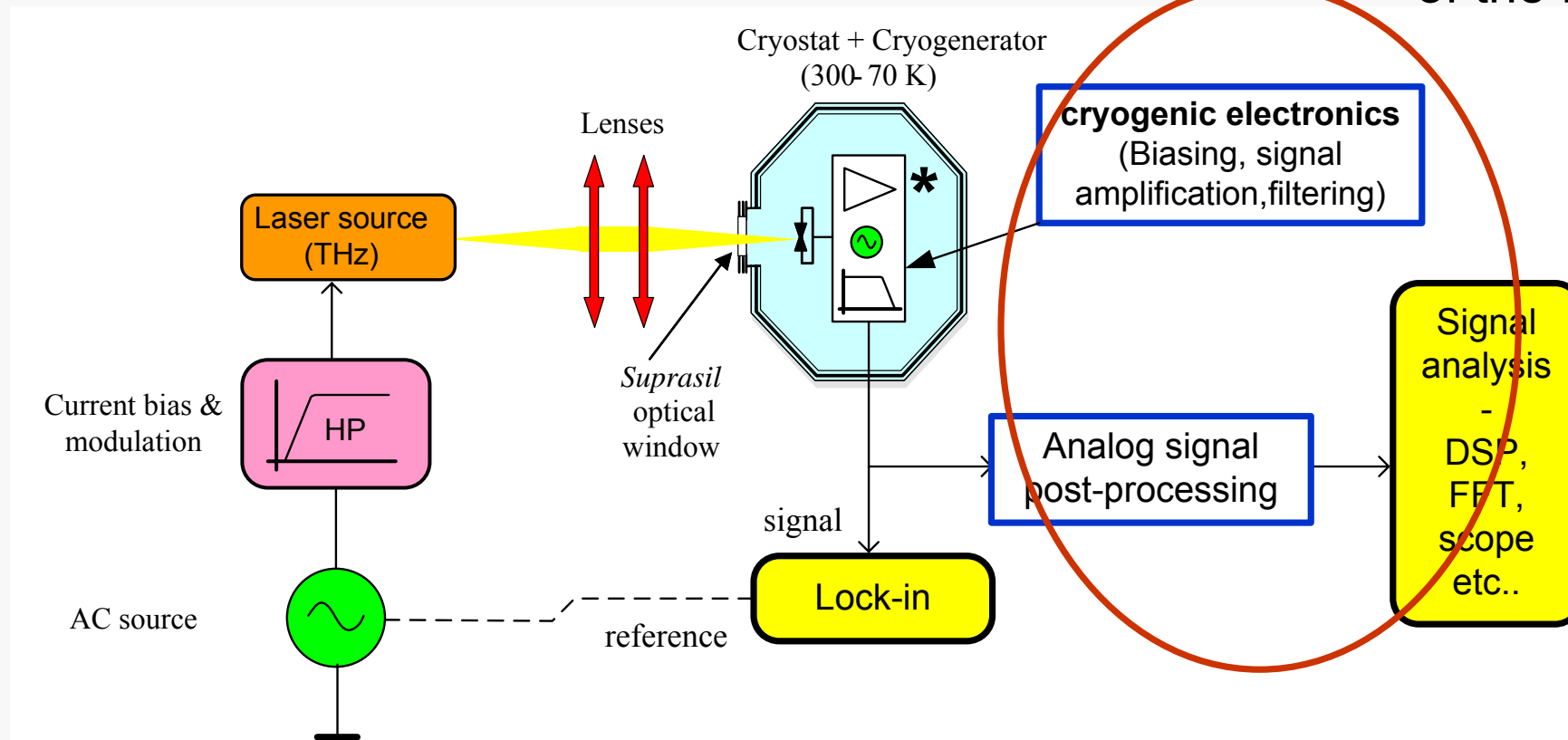
THz cryogenic test bench

do the electronics follow up?

Research objectives of PhD thesis

➔ Cryogenic integrated analog electronics for THz detection chain

➔ New structures of fixed-gain CMOS differential amplifiers; compatible with bolometric detectors at room and cryogenic temperatures

➔ High dynamic range signal processing: developpement of frequency filters with high attenuation rate
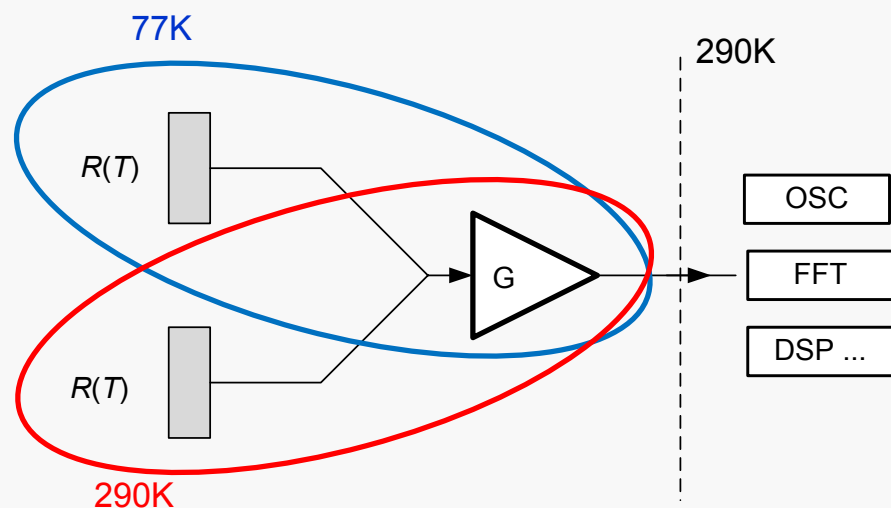
II.
Differential amplifiers for cryogenic and room temperature instrumentation
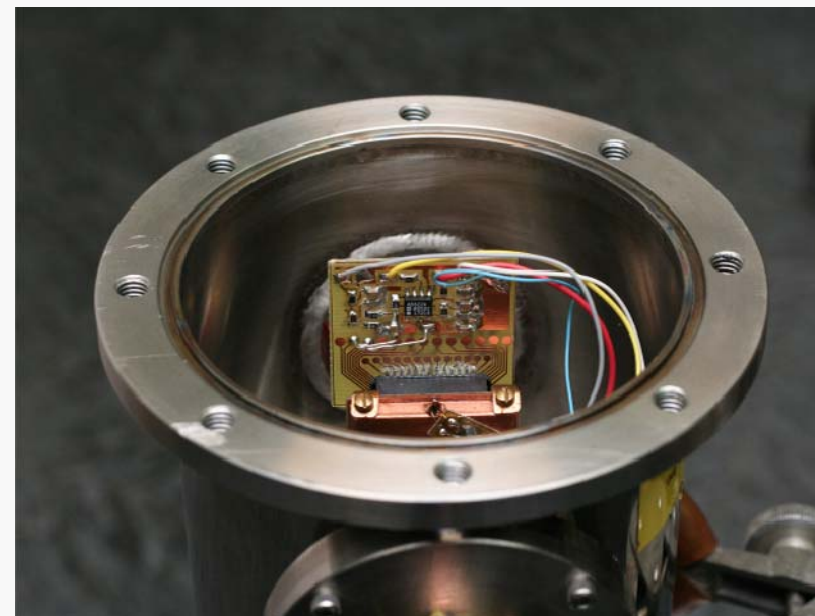
SPECIFICATIONS

Wide temperature range CMOS differential amplifiers for:

i) Room temperature (semiconducting bolometers)

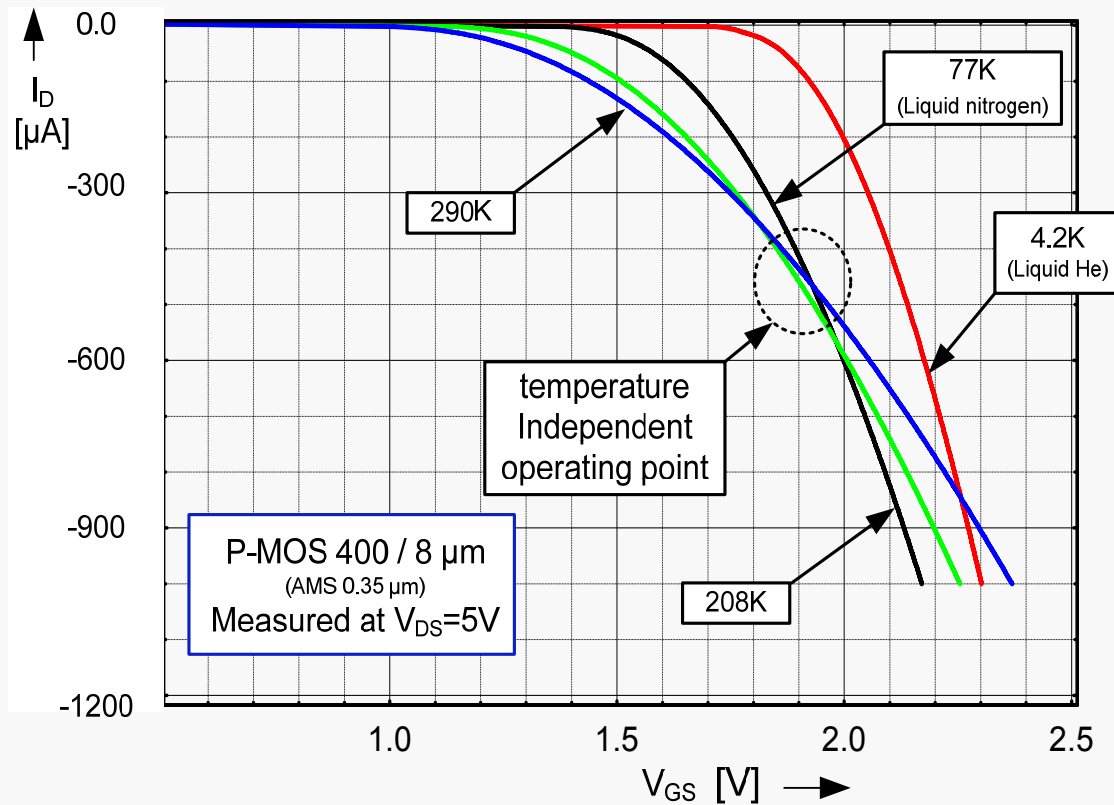*ii*) Cryogenic temperatures (high-T_C superconducting bolometers)

Requirements:

➢ 40dB, accurate gain,

➢ 70K to 300K temperature range,

➢ Differential gain BW: DC to several MHz,

➢ Low noise operation,

➢ Low power consumption,

➢ High (> 100kΩ) input impedance.

Low noise differential CMOS amplifier

MOS cryogenic modeling

Measured I-V characteristics for a PMOS 400/8μm

Measurement results obtained in
L2E UPMC – Paris 6 and CEA-INAC Grenoble

➔ Low field surface mobility:

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-x}$$

➔ Threshold voltage:

$$V_{TH}(T) = V_{TH}(T_0)\left[1 + \alpha_{THX} \cdot (T - T_0)\right]$$

➔ Analytical temperature model

$$I_D = \frac{KP}{2}\left(\frac{T}{T_0}\right)^{-x}\frac{W}{L} \cdot \left[V_{GS} - V_{TH}(T_0)\left[1 + \alpha_{THX}(T - T_0)\right]\right]^2$$

Other effects: Kink effect, mobility degradation electron freeze-out

Least squares empirical model
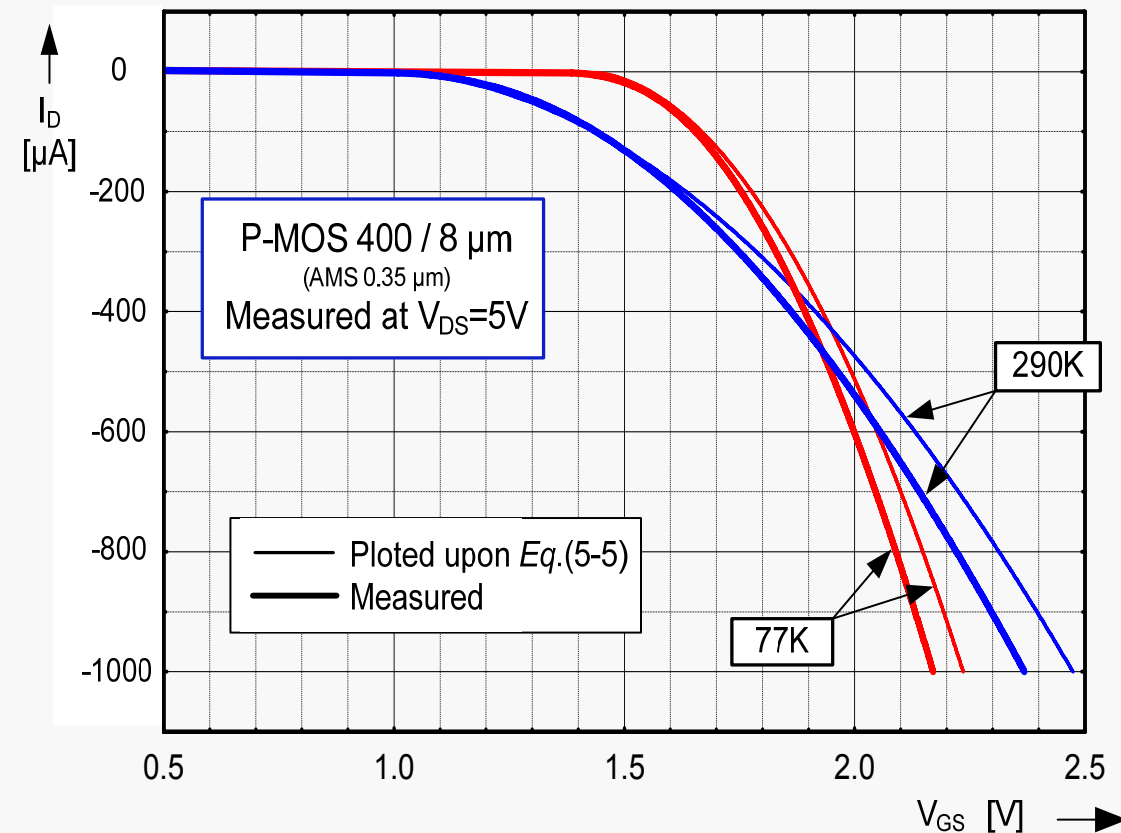
❖ LS fit of $y_i = b \cdot (x_i - a)^2$:

$$R^2 \equiv \sum_{i=0}^{n} \left[y_i - f\left(x_{1,i}, x_{2,i}...x_{m,i}, a_1, a_2...a_m \right) \right]^2 \to \min$$

$$\Rightarrow \frac{\partial R^2}{a_{1,2,..m}} = 0$$

Parameters based on LS fit (measurements and simulation SPICE-level 7)

PMOS 100/10µm	Simulation 296K	Measured 296K	Measured 77K
KP_P [A/V²]	20.6×10^{-6}	21.6×10^{-6}	72.4×10^{-6}
V_{TH}[V]	-0.96V	-0.95V	-1.405V

	x	α_{THX}	V_{TH} shift
Model coefficients	0.90	-2.16 mK⁻¹	-2.1 mV/K

P-MOS 400 / 8 µm
(AMS 0.35 µm)
Measured at V_{DS}=5V

290K

77K

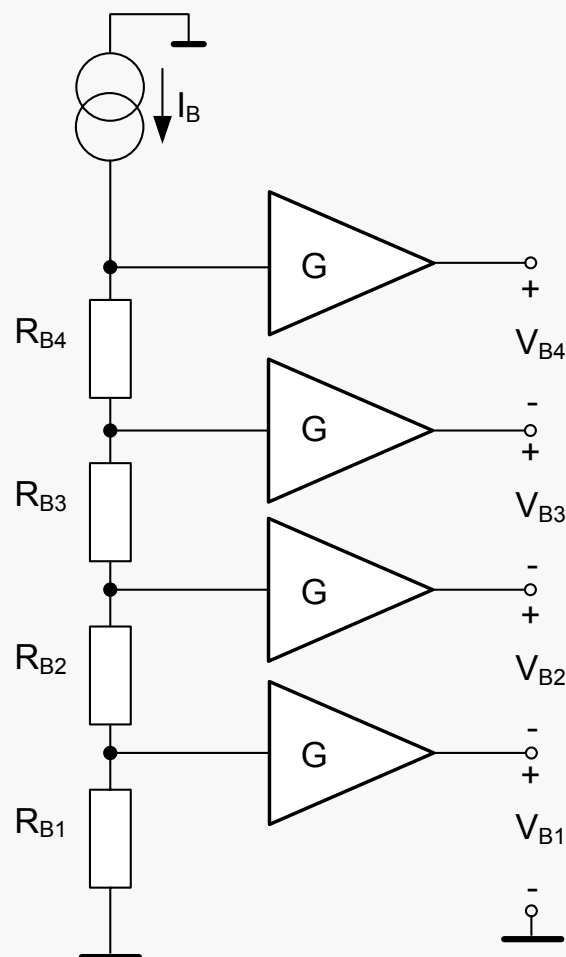— Ploted upon *Eq.*(5-5)
— Measured

I_D [µA]

V_{GS} [V]

Verification of model: different run

➔ analytical temperature model

$$I_D = \frac{KP}{2} \left(\frac{T}{T_0} \right)^{-x} \frac{W}{L} \cdot \left[V_{GS} - V_{TH}(T_0) \left[1 + \alpha_{THX} (T - T_0) \right] \right]^2$$

DC BIAS, CONFIGURATION
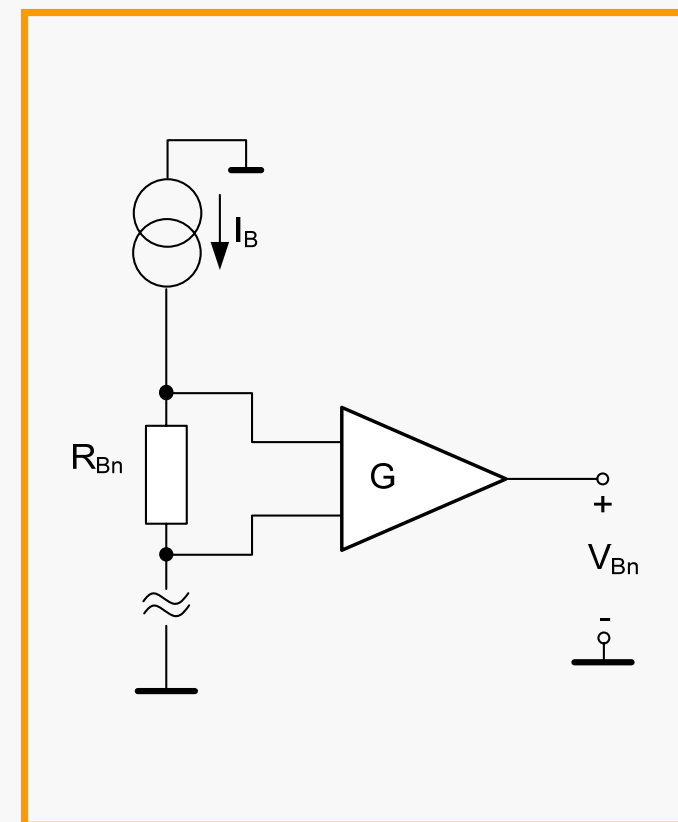

(+) **simple architecture**

(+) **low noise**

(−) **single-ended output**

(−) **DC operating point**

(−) **dynamic range**

Single-ended amplifiers [*]

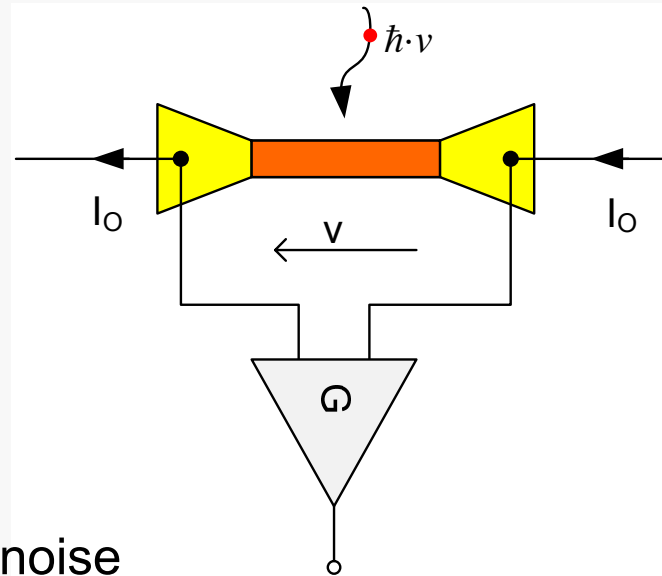[*] *PhD theses: F. Voisin, 2005, D. Prêle, 2006,*
L2E UPMC-P6

differential read-out amplifier in CMOS
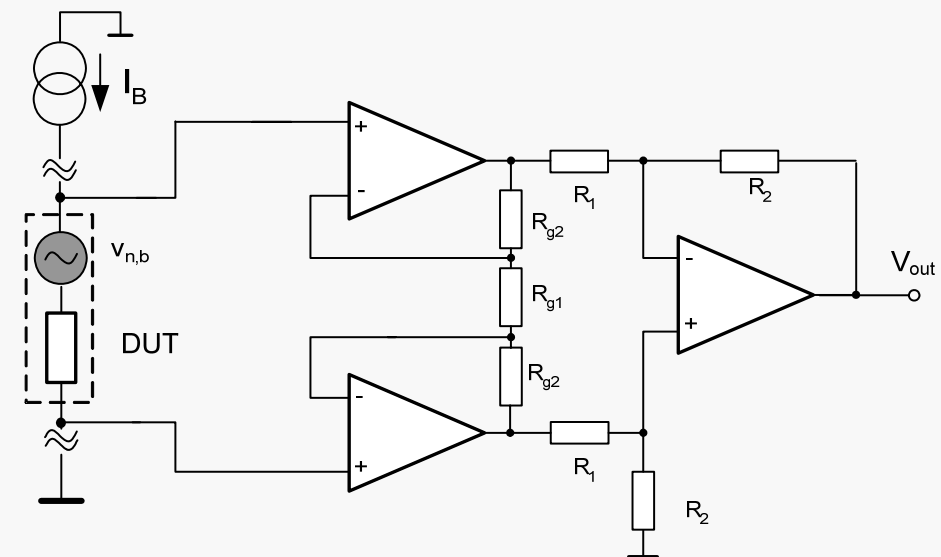
adopted solution
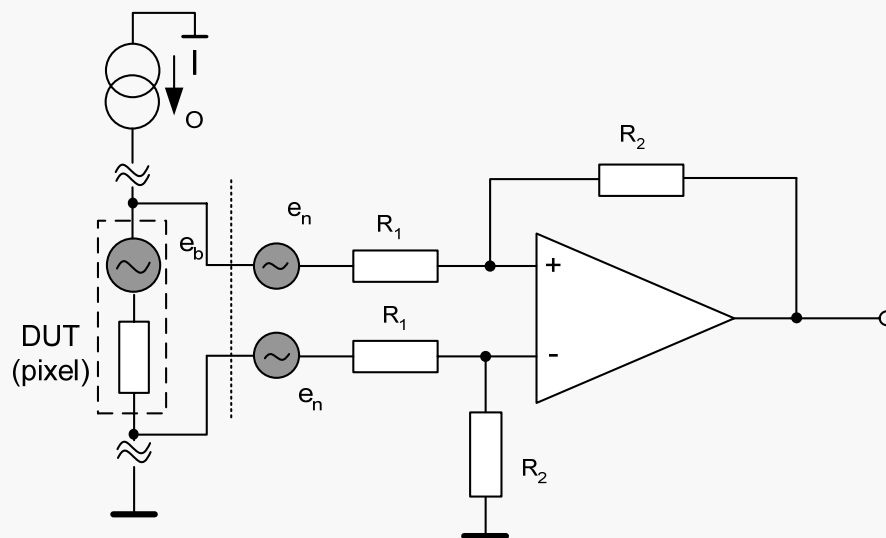
Differential amplifiers

Differential OA

- Low input impedance
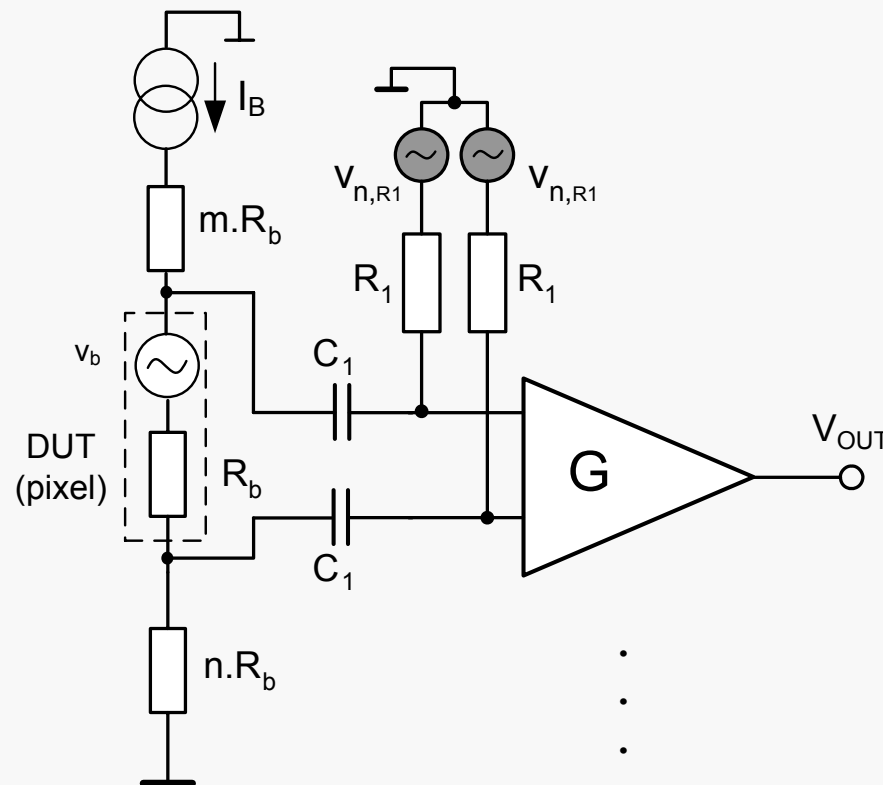- High accuracy
- Higher input referred noise

Instrumentation amplifier

- High input impedance
- Very high accuracy
- Higher input referred noise
- Low bandwidth

Solution: feedback-free amplifier

☺ **No resistors in the structure**
➔ **simplification, reduced noise, and Iq, silicon surface save**

☺ **Absence of compensation**
➔ **improves time characteristics (no stability problems) and allows to reach higher BW**

☹ **Linearity, distortion**

☹ **Missing architectures in bipolar and CMOS process**

$$v_{n,in} \cong \sqrt{\frac{8k_BT}{R_1} \cdot \left(\frac{2 + j\omega R_bC_1}{2j\omega C_1}\right)} \; {}^{*}$$
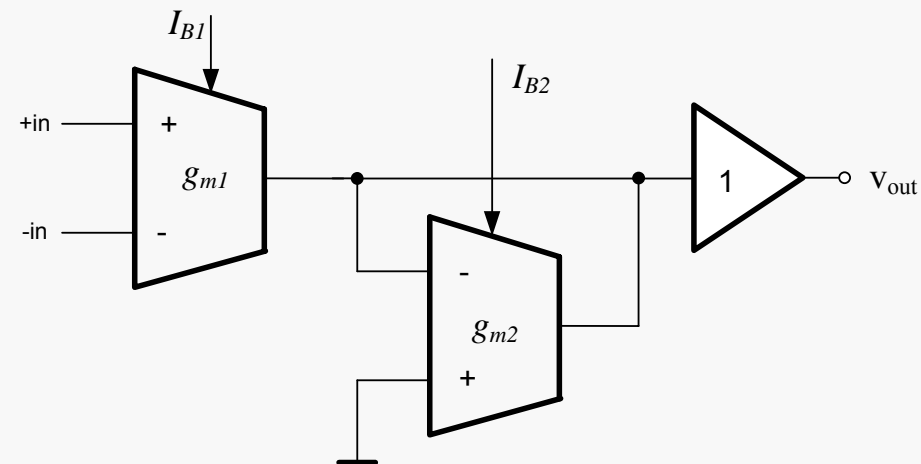
* **Bolometer noise voltage is neglected**
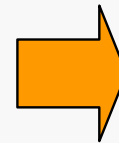
Known structures – low gain
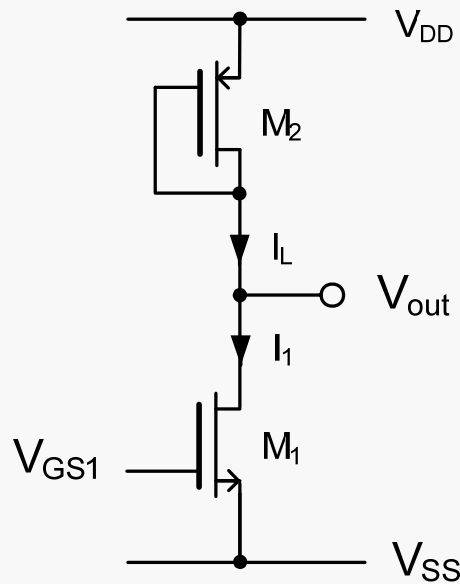
Common source MOS amplifier

OTA-based differential fixed-gain amplifier

The expression of the gain follows a square-root law:

$$G_0 = \frac{dV_{OUT}}{dV_{GS1}} = -\sqrt{\frac{KP_N}{KP_P}} \sqrt{\frac{W_1/L_1}{W_2/L_2}}$$

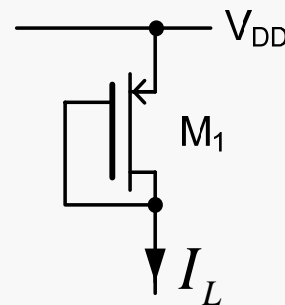For 40 dB, the $(W/L)_1 / (W/L)_2$ as high as 10 000·KP_P/KP_N

Adopted technique: low g_m load

Voltage gain fixed in the structure by the transconductance ratio

$$G_0 = \frac{g_{m1}}{g_{m2}}$$

Active loads

MOS diode

V_{DD}

M_1

I_L

$$g_m = \sqrt{2KP\frac{W}{L}I_L}$$

$$g_m' = \sqrt{2KP \cdot \frac{W_1}{L_1}\left(I_L - I_{M2}\right)}$$

Decreasing the transconductance by current sink

PhD F. Voisin, 2005, L2E-LISIF

V_{DD}

M_1

M_2

V_{BIAS}

I_{M2}

I_L

Current difference makes the function very sensitive:

$$S_k^{g_m'} = \frac{\partial g_{m(k)}'}{\partial k} \cdot \frac{k}{g_{m(k)}'} = -\frac{1}{2}\frac{k}{1-k}$$
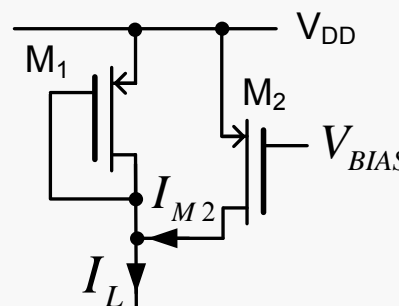
Proposed low g_m composite transistor

$\alpha_2 \quad : \quad 1$

V_{DD}

M_1 $\quad$ M_5

I_L

v_{out}

M_2

i_2 $\quad$ i_4

$+$

v_L

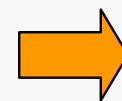M_3 $\quad$ M_4

$-$

V_{SS}

$1 \quad : \quad \alpha_1$
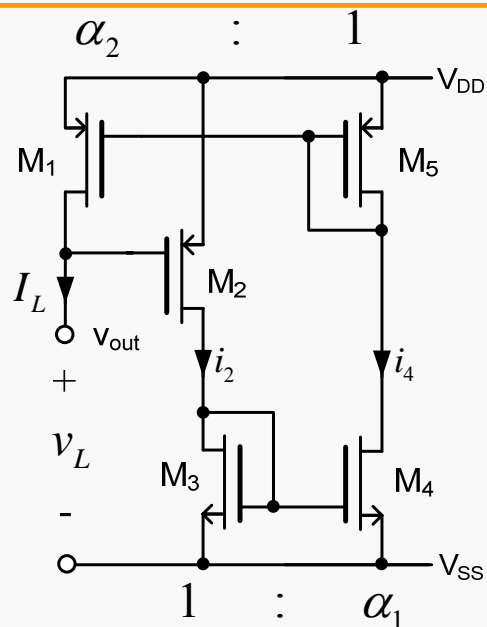
***Proposed method* for decreasing**
the transconductance by means of
current scaling:

$$g_m' = \sqrt{2 \cdot KP_{(T_2)} \cdot \frac{W_2}{L_2} \cdot \left(\frac{\dfrac{W_4}{L_4} \cdot \dfrac{W_1}{L_1}}{\dfrac{W_3}{L_3} \cdot \dfrac{W_5}{L_5}} \right) \cdot I_L}$$
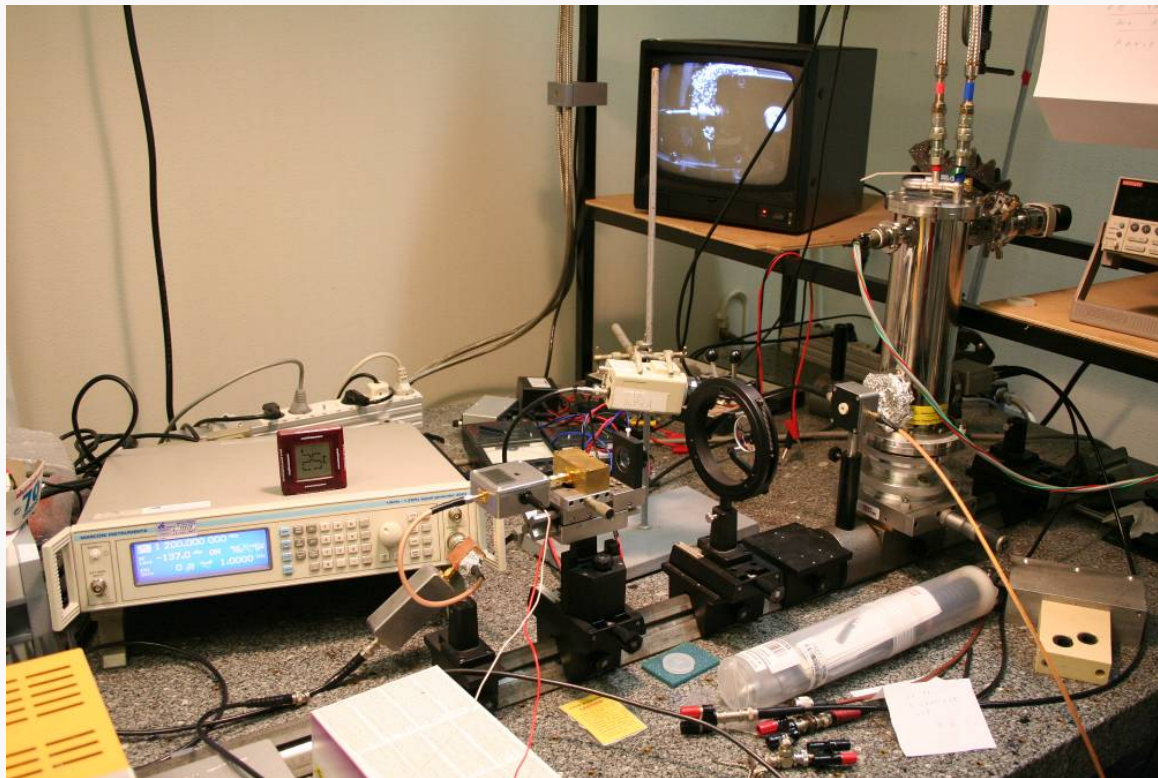

Inaccurate

accurate

$$g_m' = \frac{i_L}{v_L} = g_{m2} \cdot \frac{g_{m4} \cdot g_{m1}}{g_{m3} \cdot g_{m5}} = \alpha_1 \cdot \alpha_2 \cdot g_{m2}$$
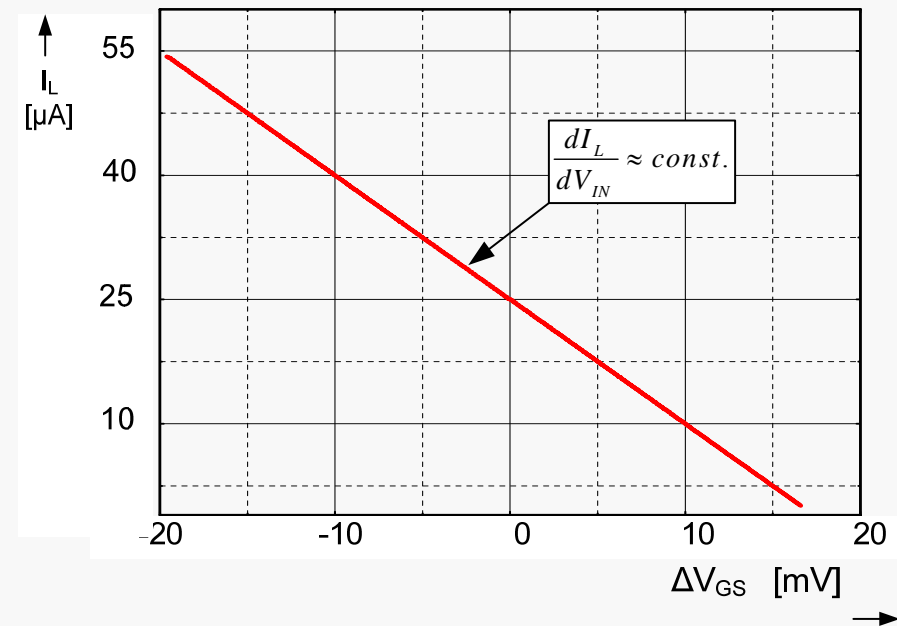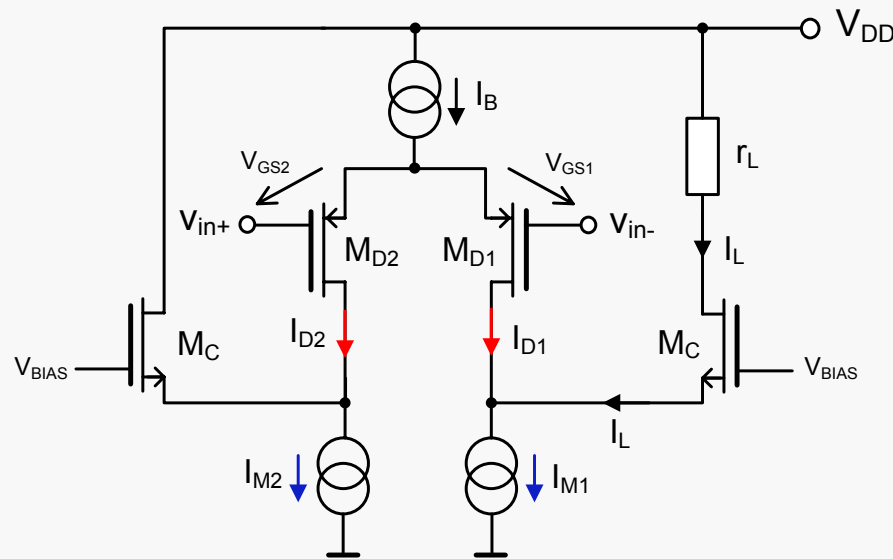
II.1
1st folded cascode
CMOS amplifier
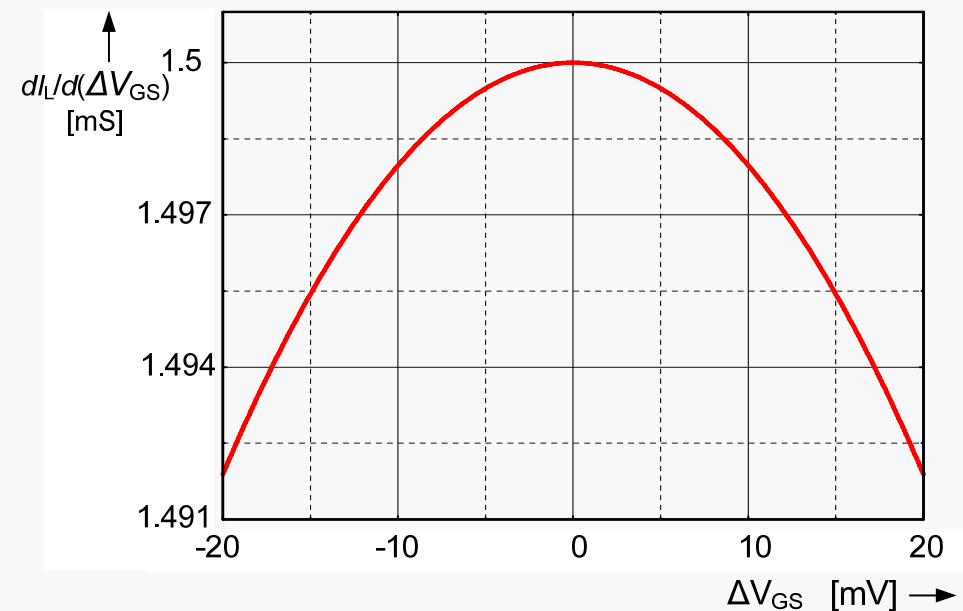
Folded cascode OTA: analysis

➔ **DC characteristic:**

$$I_{D1} = \frac{1}{8} \cdot \left(\sqrt{4 \cdot I_B - KP \cdot \frac{W_D}{L_D} \cdot \Delta V_{GS}^2} + \sqrt{KP \cdot \frac{W_D}{L_D} \cdot \Delta V_{GS}} \right)^2$$
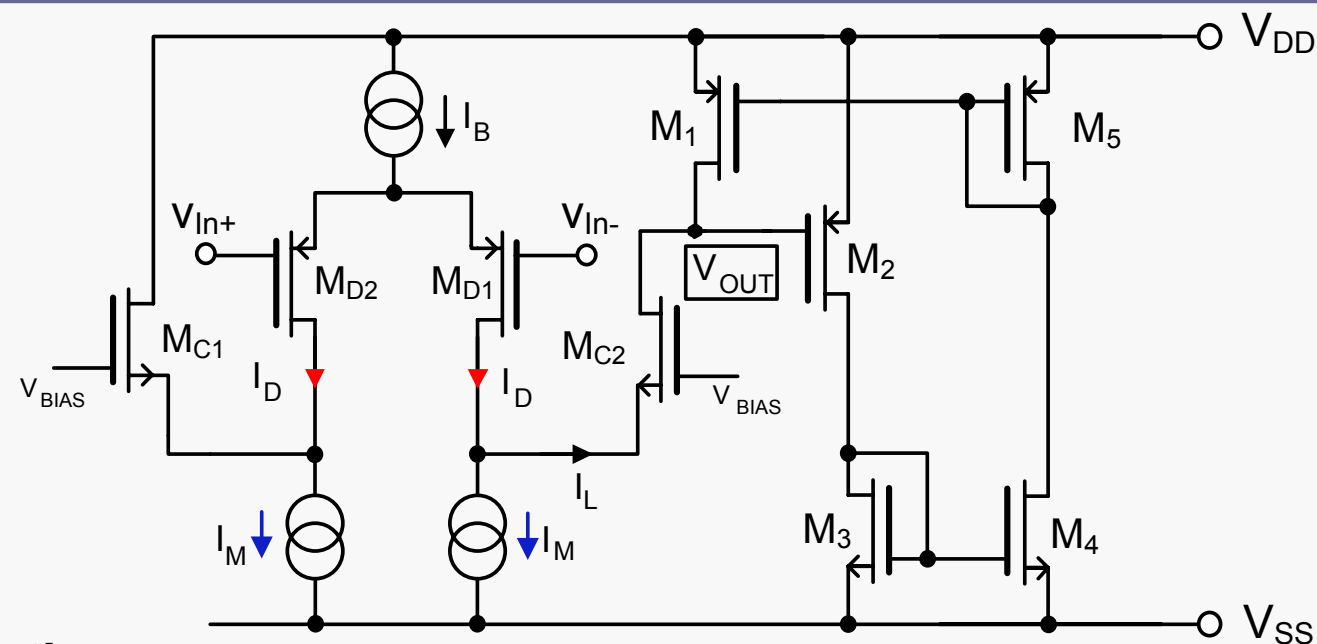
➔ **g_m:**

$$g_{mDiff} = \frac{dI_{D1}}{d\Delta V_{GS}}\bigg|_{\Delta V_{GS}=0} = \frac{1}{2} \cdot \sqrt{KP_P \cdot \frac{W_D}{L_D} \cdot I_B}$$

The stage behaves as a quasi-linear current source

Proposed 1st folded cascode amplifier

➢ **DC transfer characteristic:**

$$V_{OUT} = V_{DD} - |V_{TH,P}| - \sqrt{\frac{2}{KP_P \cdot \left(\frac{W_2}{L_2}\right)} \cdot \left(\frac{\frac{W_3}{L_3} \cdot \frac{W_5}{L_5}}{\frac{W_4}{L_4} \cdot \frac{W_1}{L_1}}\right) \cdot \left[I_{M1} - \frac{1}{8} \cdot \left(\sqrt{4 \cdot I_B - KP_P \cdot \frac{W_D}{L_D} \cdot \Delta V_{GS}^2} + \sqrt{KP_P \cdot \frac{W_D}{L_D}} \cdot \Delta V_{GS} \right)^2 \right]}$$
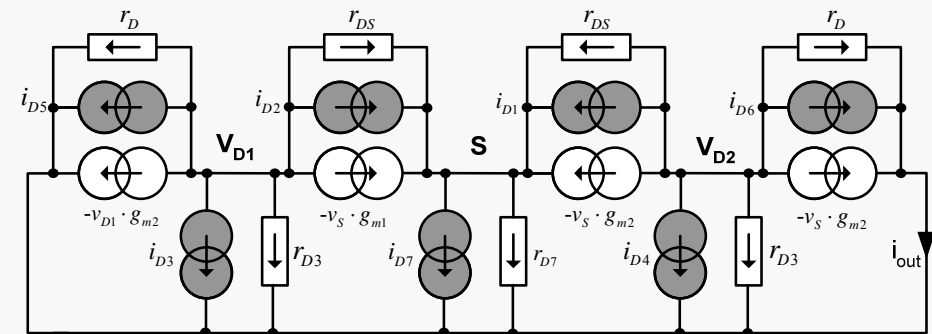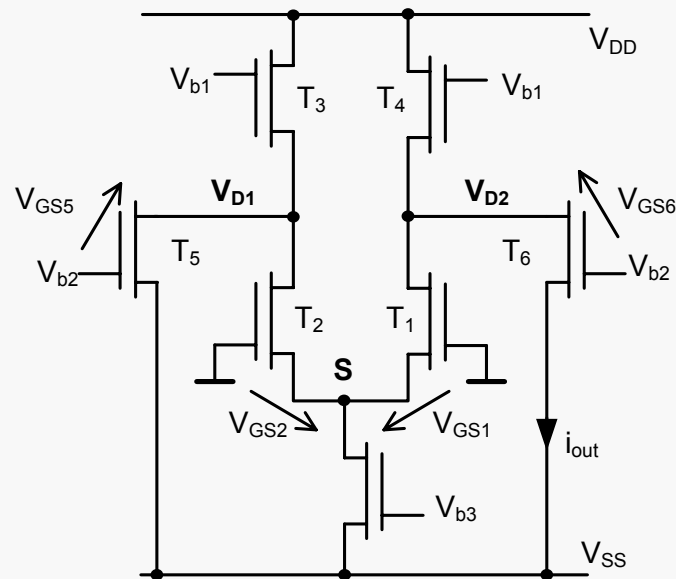
➢ **Gain is the slope of DC transfer characteristic:**

$$\boxed{G_0 = \frac{dV_{out}}{d\Delta V_{GS}}\bigg|_{\Delta V_{GS}=0} = \frac{1}{2}\sqrt{\frac{L_{eff}}{W_{eff}} \cdot \frac{W_D}{L_D}} \cdot \sqrt{\frac{I_B}{2 \cdot I_{L(\Delta V_{GS}=0)}}},}$$

where:

$$\frac{W_{eff}}{L_{eff}} = \frac{\frac{W_2}{L_2} \cdot \frac{W_4}{L_4} \cdot \frac{W_1}{L_1}}{\frac{W_3}{L_3} \cdot \frac{W_5}{L_5}}$$
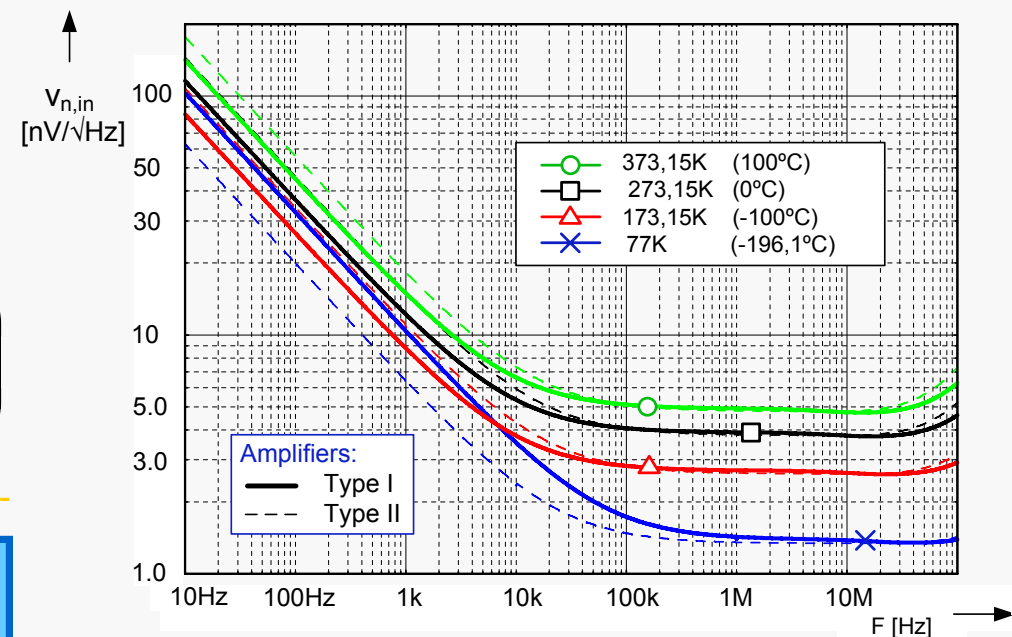
Noise analysis of folded cascode

Small signal equivalent circuit

The equivalent input noise:

$$\overline{e}_{in}^2 = \frac{\overline{e}_{OUT}^2}{G^2} = \frac{8}{3} k_B T \left(\frac{1}{2} \cdot \frac{1}{g_{mdiff}} + \frac{1}{4} \cdot \frac{g_{m7}}{g_{mdiff}^2} + \frac{g_{m4}}{g_{mdiff}^2} \right)$$
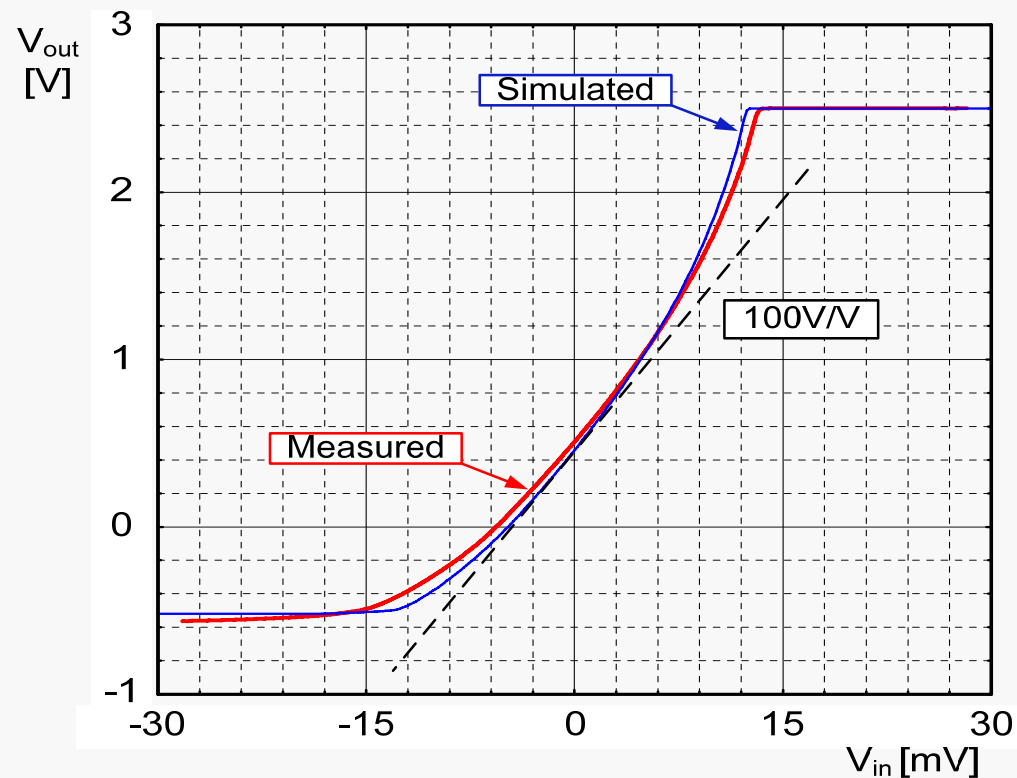
A very low thermal noise is observed at cryogenic temperature (T = 77 K):
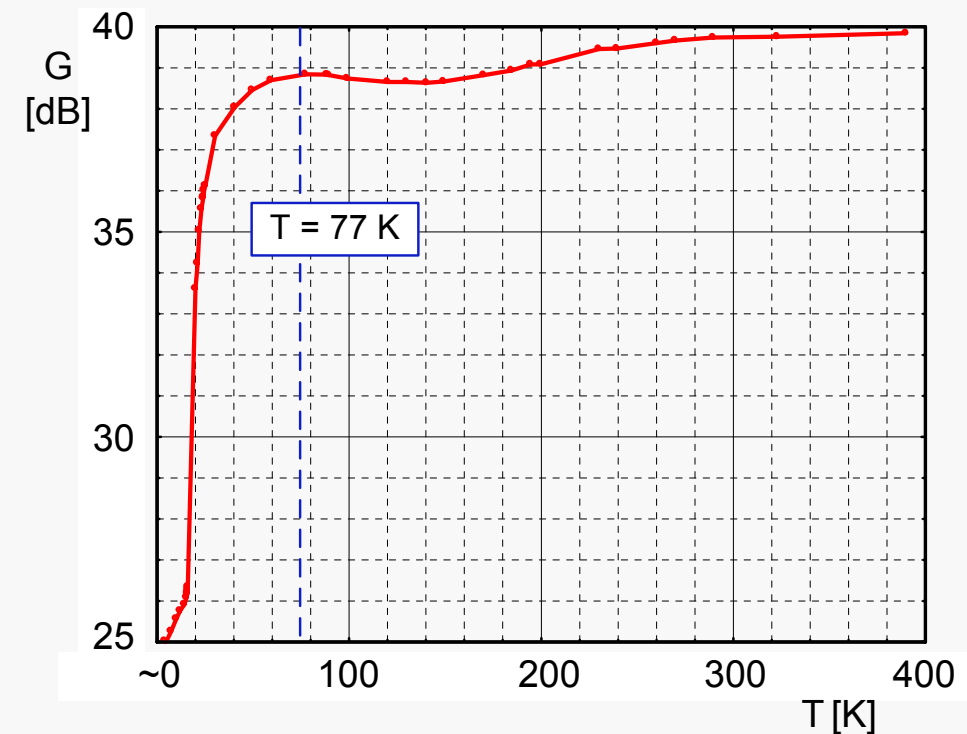
$$v_{n,in} = 1.5 \ nV/\sqrt{Hz}.$$

Simulated input-referred noise voltage (both amplifiers)

Measurements: wide temperature results

DC transfer characteristic at T = 290K

Temperature function of voltage gain

CMOS: AMS 0.35 µm

Results DC and AC characteristics

Amplifier	Gain [dB]
A$_5$	**39.84**
A$_{5\_2}$	39.75
A$_1$	40.10
A$_2$	39.62
A$_3$	39.52
A$_4$	39.85
AVG	39.78

Dispersion *of voltage gain*
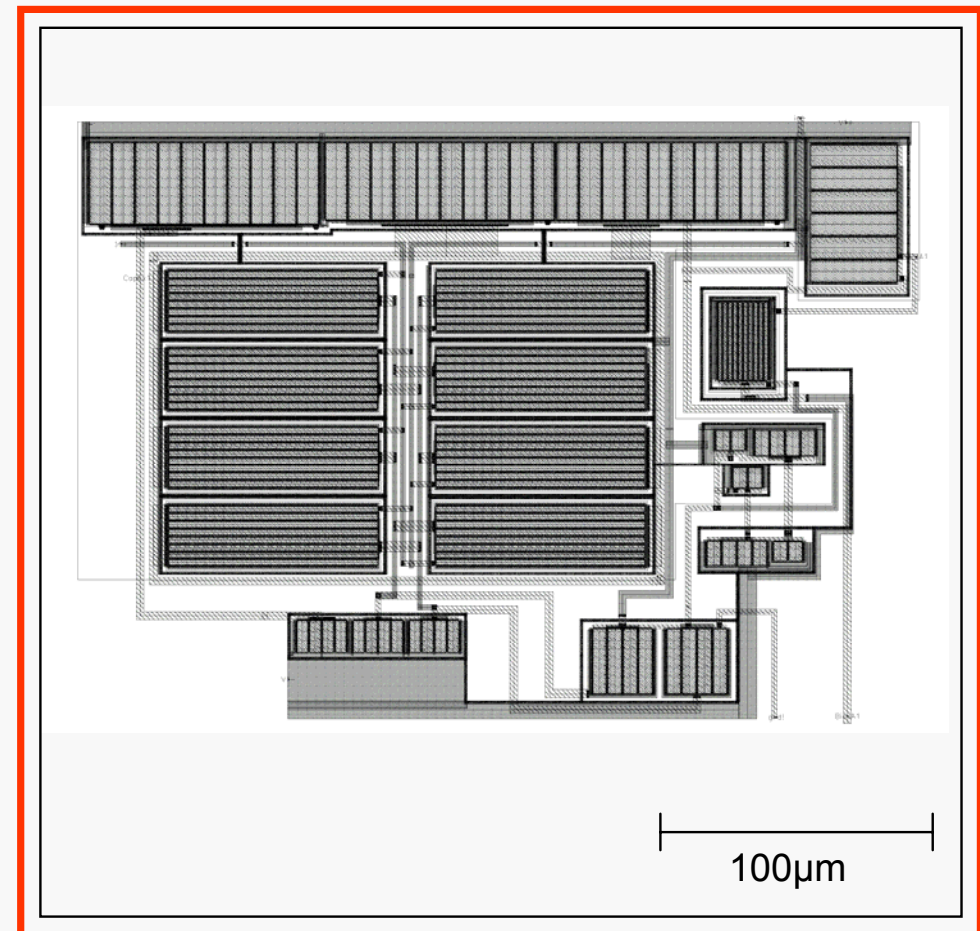*(A$_{5\_2}$ refers to chip 2)*
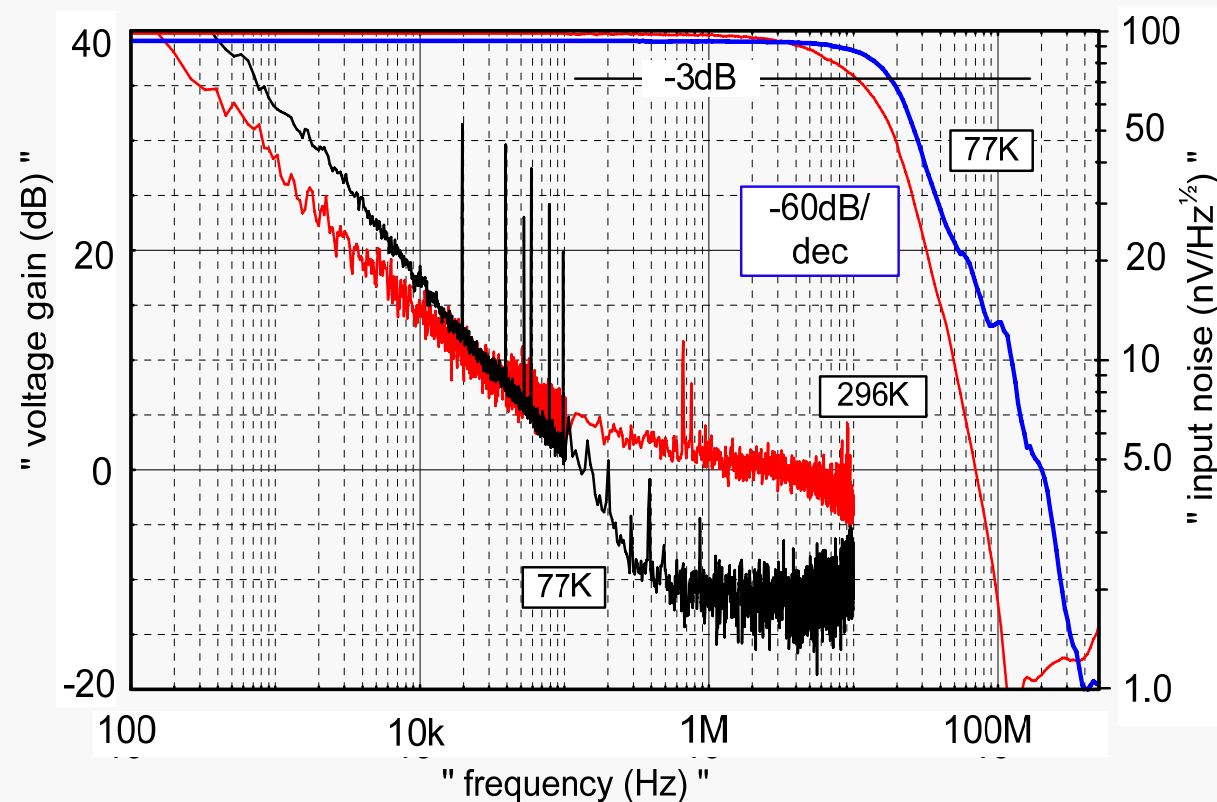
AC response and input noise (V$_{DD}$=5V, I$_Q$=2mA)

1st amplifier: summary

- **New amplifier architecture for extreme temperature range**

- **State-of-the-art: low noise and large BW operation (up to 1.7GHz GBW at Iq = 2.1mA)**

- **Gain is fixed by means of geometric ratio: no variation with temperature**

- **Sufficient linearity for small signals: DC characteristic $\propto \sqrt{}$ Vin**

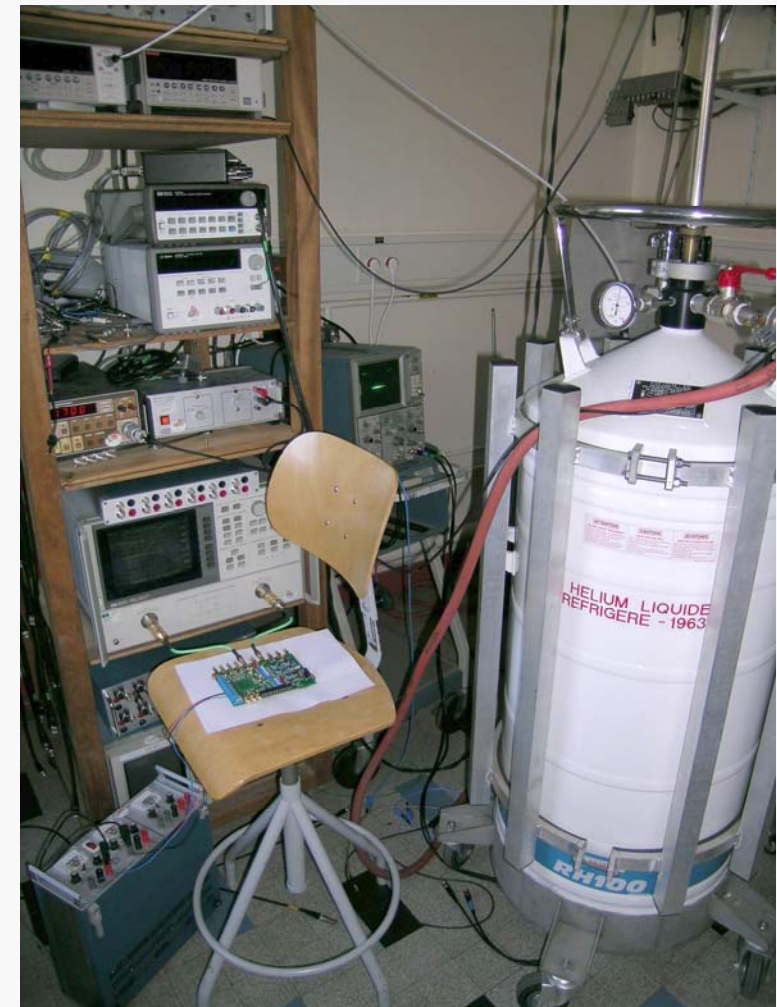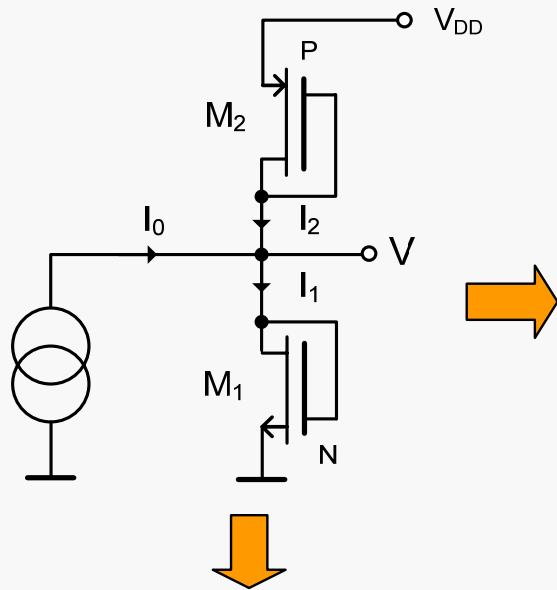100µm

Layout in CMOS 0.35µm AMS process

V. Michal et al. "*Fixed-gain CMOS differential amplifiers with no external feedback for a wide temperature range*", Cryogenics (2009)

II.2
2st amplifier: linearization and temperature compensation

2nd amplifier: new temperature compensation and linearization

Based on **cancelling the quadratic terms**. The node equation can be written:

$$\frac{\beta_1}{2}\left(V - V_{TH1}\right)^2 = \frac{\beta_2}{2}\left(V_{DD} - V - \left|V_{TH2}\right|\right)^2 + I_0$$
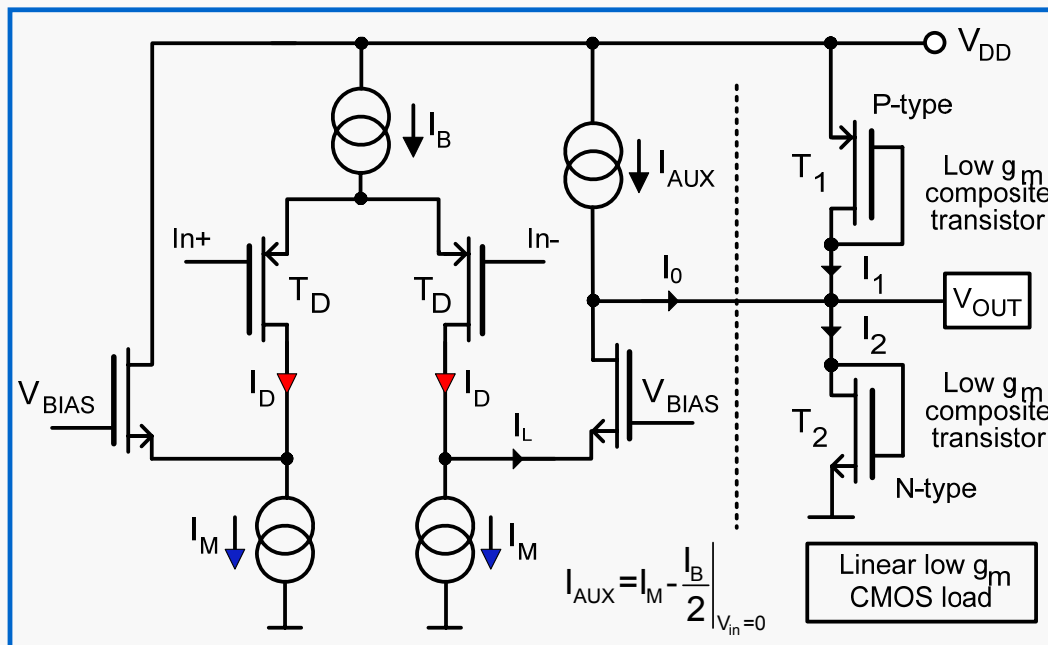
The extraction of output voltage leads to (assuming $\beta_1 = \beta_2$, $V_{TH1} = V_{TH2}$):

$$V = \frac{V_{DD}}{2} + \frac{I_0}{\beta(V_{DD} - 2 \cdot |V_{TH}|)}$$

$I_{AUX} = I_M - \left.\frac{I_B}{2}\right|_{V_{in}=0}$

Linear low g$_m$ CMOS load

Condition: $\beta_1=\beta_2$, $V_{TH1}=V_{TH2}$: solution
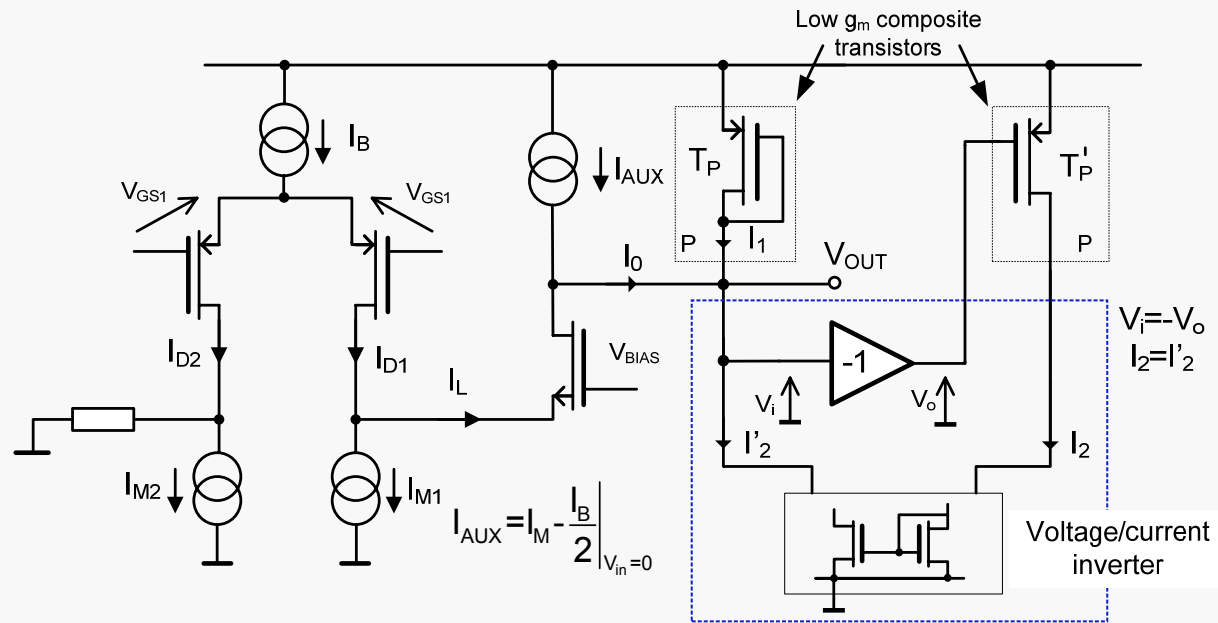
Symmetrisation of the low g_m linear load

Single well
Symmetric low-g_m CMOS load

Analysis of DC transfer

➡ **DC transfer function:**

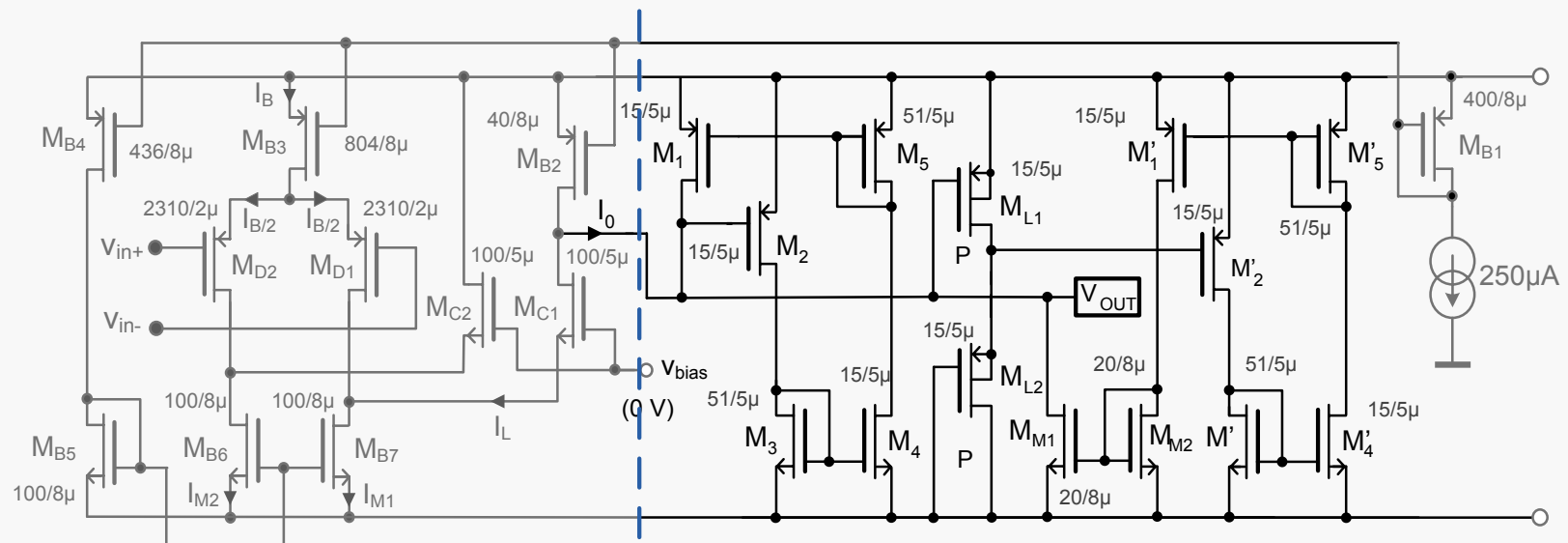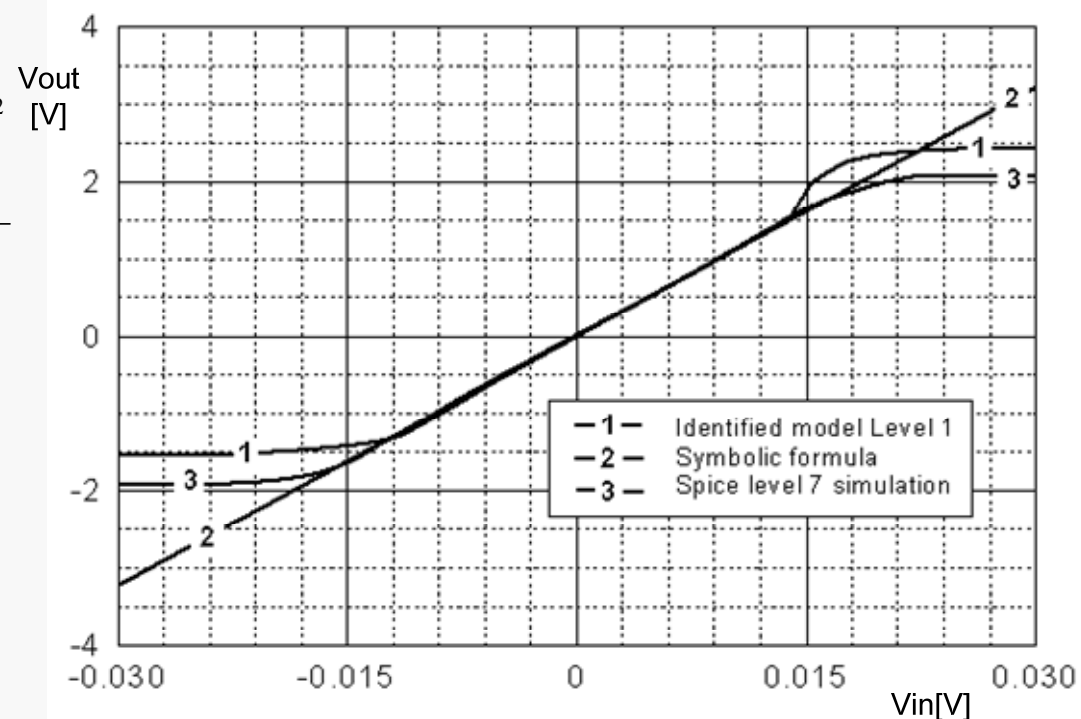$$V_{out} = \frac{1}{2}V_{DD} + \frac{\dfrac{1}{2}I_B - \dfrac{1}{8}\left(\sqrt{4\cdot I_B - KP_P \cdot \dfrac{W_D}{L_D}\cdot\Delta V_{GS}^2} + \sqrt{KP_P\cdot\dfrac{W_D}{L_D}\cdot\Delta V_{GS}}\right)^2}{KP_P\cdot\dfrac{W_{eff}}{L_{eff}}\left(V_{DD} - 2\cdot\left|V_{TH,P}\right|\right)}$$

➡ **Gain is given by derivative:**

$$G_0 = \left.\frac{dV_{out}}{d\Delta V_{GS}}\right|_{\Delta V_{GS}=0} = \frac{1}{2}\cdot\frac{\sqrt{I_B\cdot\dfrac{W_D}{L_D}}}{\sqrt{KP_P}\cdot\dfrac{W_{eff}}{L_{eff}}\cdot\left(V_{DD} - 2\cdot\left|V_{TH,P}\right|\right)}$$

DC transfer characteristics

The voltage gain as the function of:

- $\sqrt{(W/L)_D/(W/L)_{eff}}$ ratio,
- Technological parameters: $\sqrt{KP_P}$, V_{THP}.
- Bias current I_B and power supply voltage V_{DD}.

$S_{x_i}^{G_r}$	KP	V$_{TH}$	V$_{DD}$	I$_B$	W$_D$/L$_D$	W$_{Eff}$/L$_{Eff}$
	$-\dfrac{1}{2}$	$\dfrac{2\cdot V_{THP}}{V_{DD}-2\cdot V_{THP}}$	$-\dfrac{V_{DD}}{V_{DD}-2\cdot V_{THP}}$	$\dfrac{1}{2}$	$\dfrac{1}{2}$	-1

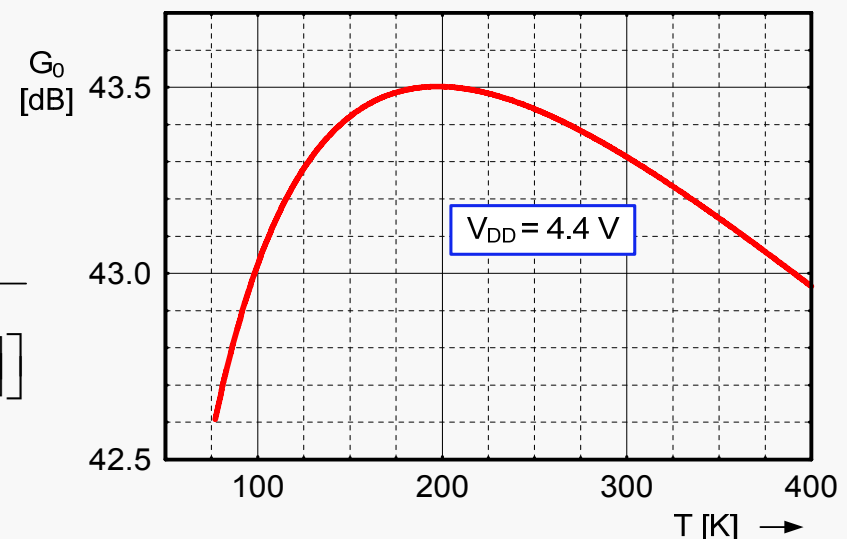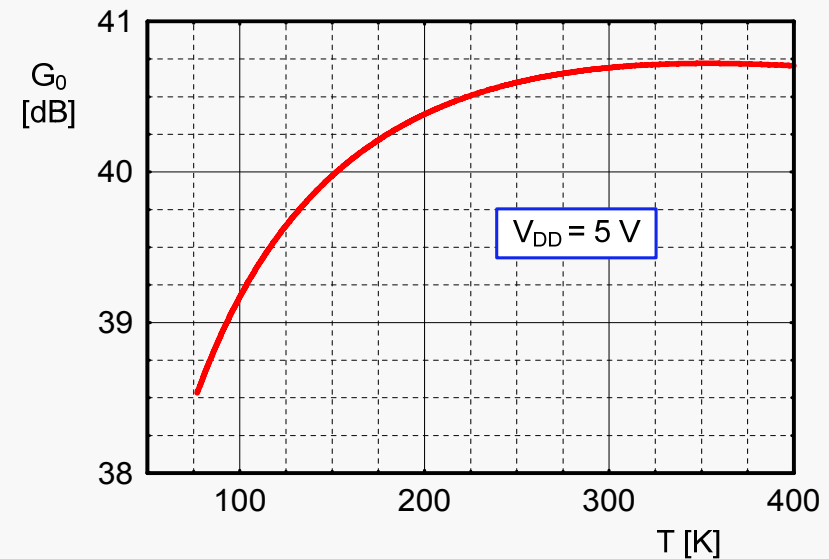# Temperature compensation principle: current / voltage biasing

➜ **Voltage gain :**

$$G_0 = \frac{dV_{out}}{d\Delta V_{GS}}\bigg|_{\Delta V_{GS}=0} = \frac{1}{2} \cdot \frac{\sqrt{I_B \cdot \dfrac{W_D}{L_D}}}{\sqrt{KP_P} \cdot \dfrac{W_{eff}}{L_{eff}} \cdot \left(V_{DD} - 2 \cdot |V_{TH,P}|\right)}$$

➜ **We replace the elements without temperature dependence by *C*:**
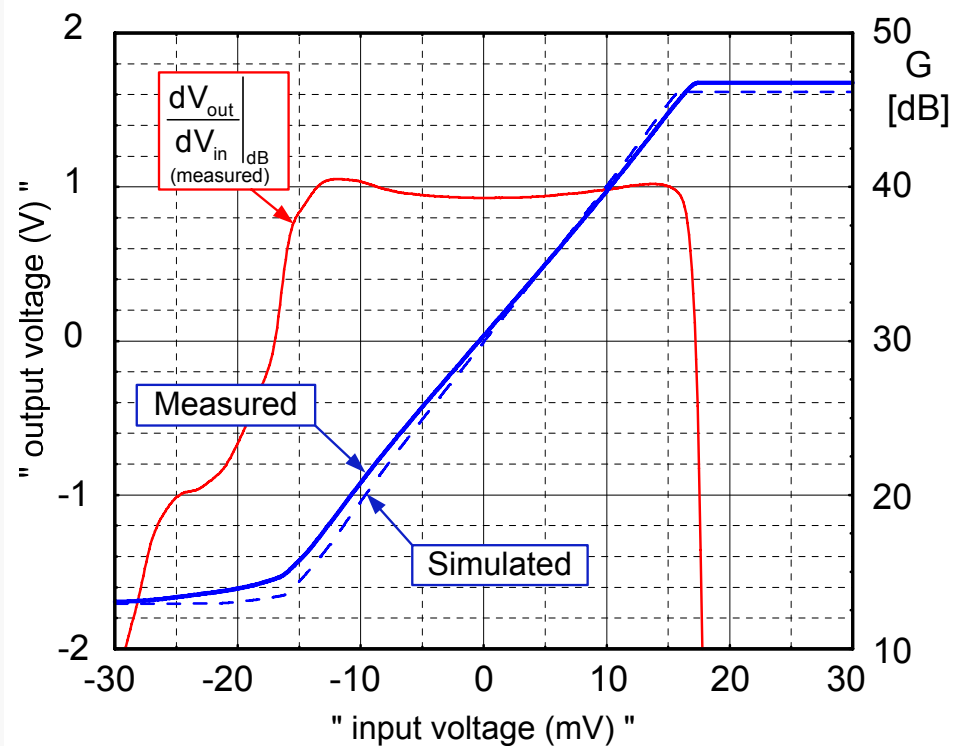
$$G_0(T) = \frac{C}{\sqrt{KP_P(T)} \cdot \left(V_{DD} - 2 \cdot |V_{TH,P}(T)|\right)}$$

➜ **Which leads to:**

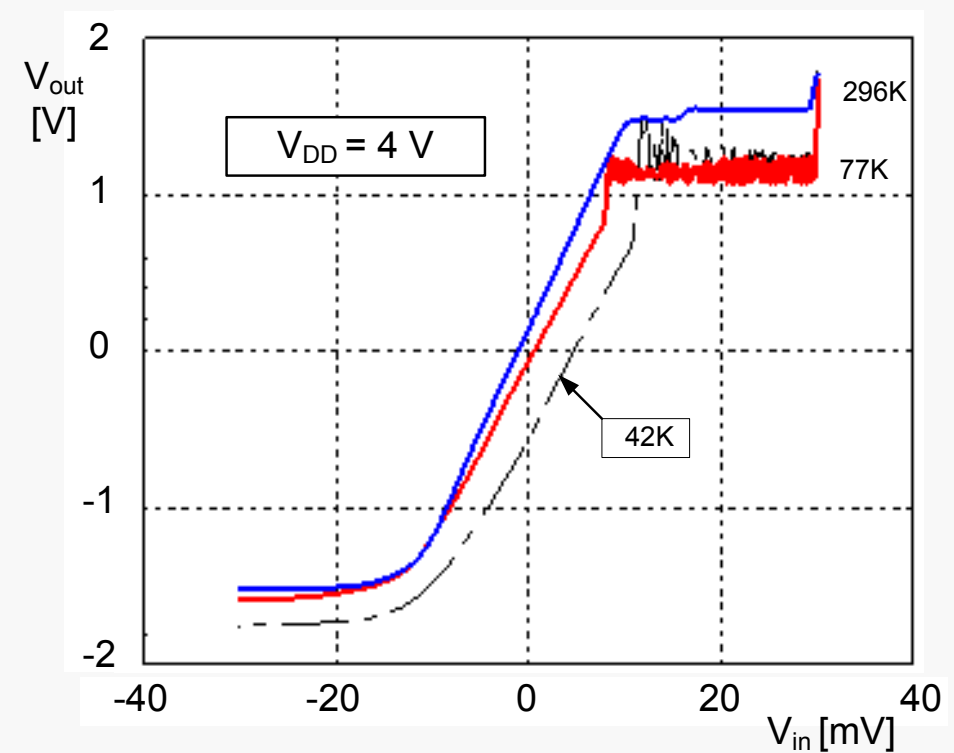$$\frac{G_0(T)}{C} = \frac{1}{\sqrt{\mu_P(T_0) \cdot \left(\dfrac{T}{T_0}\right)^{-x}} \cdot \left[V_{DD} - 2 \cdot |V_{TH,P}(T_0)| \left[1 + \alpha_{THX} \cdot (T - T_0)\right]\right]}$$

G_0 [dB]

$V_{DD} = 5\ V$

T [K]

G_0 [dB]

$V_{DD} = 4.4\ V$

T [K]

Measurements: wide temperature range
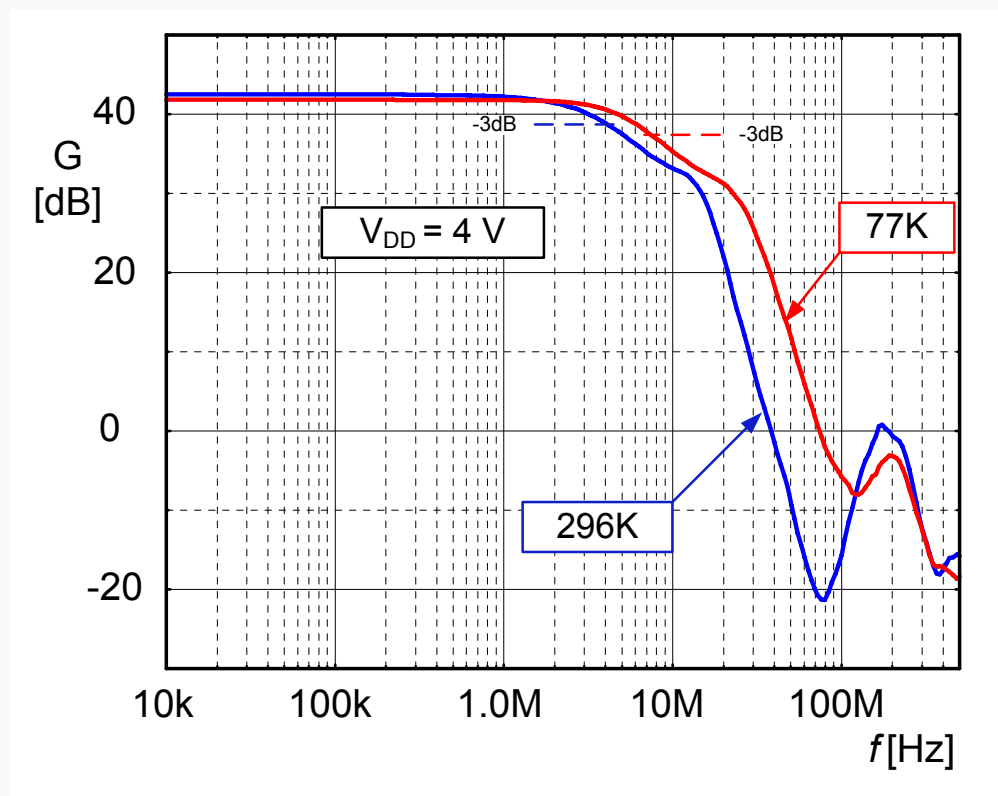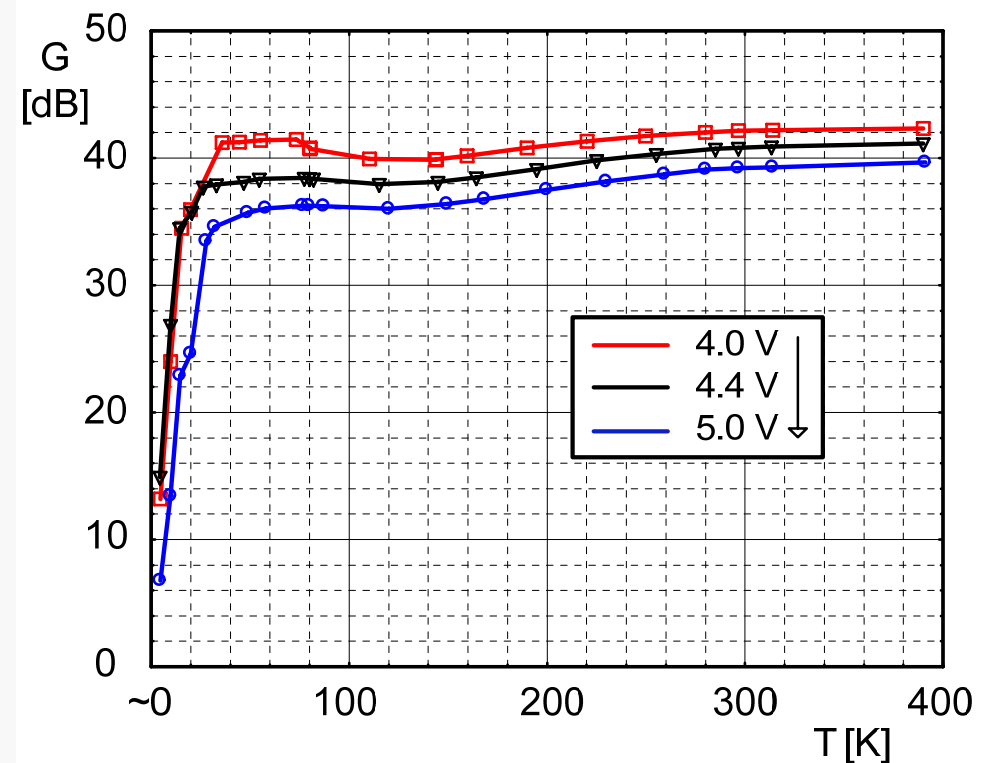

DC transfer characteristic at T = 290K

DC transfer characteristic at T = 290 and 77K

CMOS: AMS 0.35 μm

Measurements: wide temperature range

AC transfer @ 2.5V, 290 and 77 K

Temperature gain function for three V_{DD} voltages

2st amplifier: summary

- **New** amplifier architecture **for extreme temperature range**

- **Wide** linear **operation, temperature compensation**

- **Low noise, wide BW achieved with low Iq (Up to** 1GHz GBW **for 1.3 mA quiescent current)**

- Highly competitive **with bipolar amplifiers, promising as compact cell for VLSI integration**

100µm

Layout in CMOS 0.35µm AMS process

V. Michal et al. "*Fixed-gain CMOS differential amplifiers with no external feedback for a wide temperature range*", Cryogenics (2009).
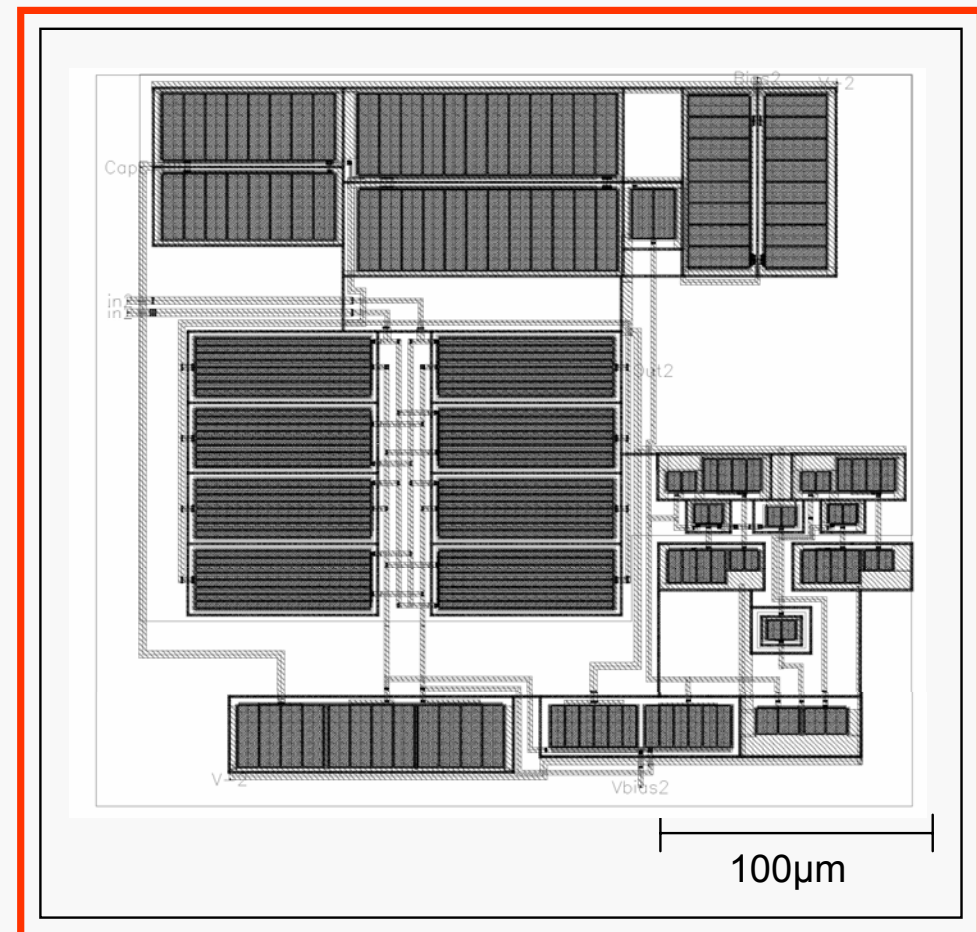
III.
High performance analog frequency filters
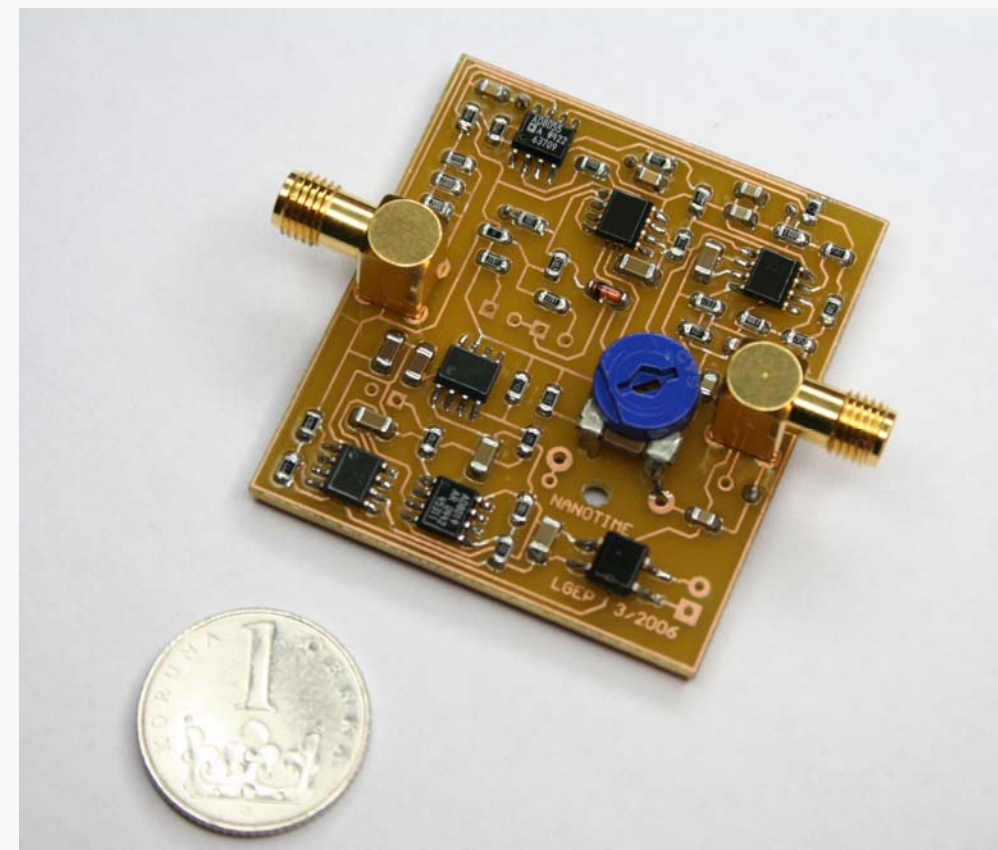
Motivation

* Correct analog processing close to the physical sensor is the best way to condition the signal

* Noise reduction is based on the spectrum reduction (Lock-in, FFT …)

* Frequency filters: crucial block

➔ **Objectives:**

  * Optimization of the dynamic range (attenuation)

  * Mastering of the topic, related work not presented in the thesis (goal-directed lossy active filters [*], adaptive analog signal processing [**], microwave superconducting filters [***])

[*] V. Michal et al. "*Active filters based on goal-directed lossy RLC prototypes* ", Speto int conference (2006)

[**] V. Michal et al. "*The analog filter design and Interactive analog signal processing by PC*" WSEAS (2005)

[***] V. Michal et al. "*Superconducting NbN band-pass filter and Matching circuit for 30GHz RSFQ Data Converters* ", IEEE conference Radioelek, 2009
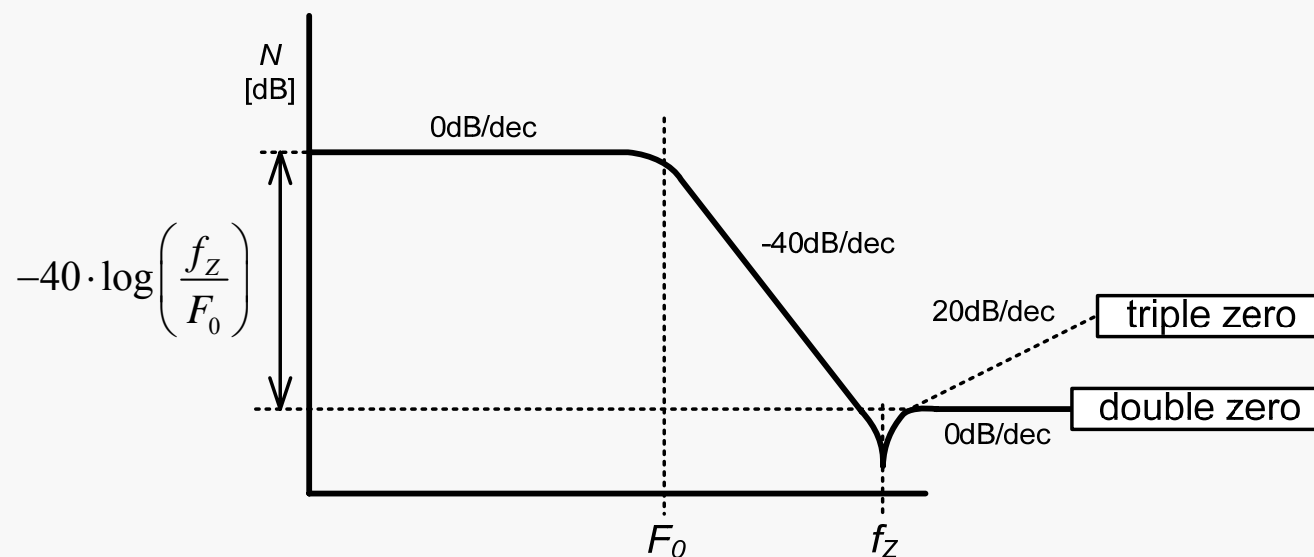
Real-world frequency filters

❖ Non-ideal passive components:

  ▪ f_0,Q inaccuracy, higher order effects, can be compensated [*]

❖ Non ideal active components

  ▪ f_0,Q inaccuracy, DC offset, <u>attenuation</u>

$$-40 \cdot \log\left(\frac{f_Z}{F_0}\right)$$

0dB/dec

−40dB/dec

20dB/dec — triple zero

double zero

0dB/dec

F_0 f_Z
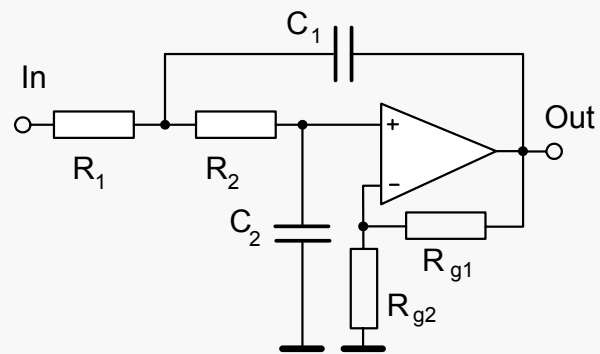
Parasitic zeros cannot be compensated by predistortion [**]

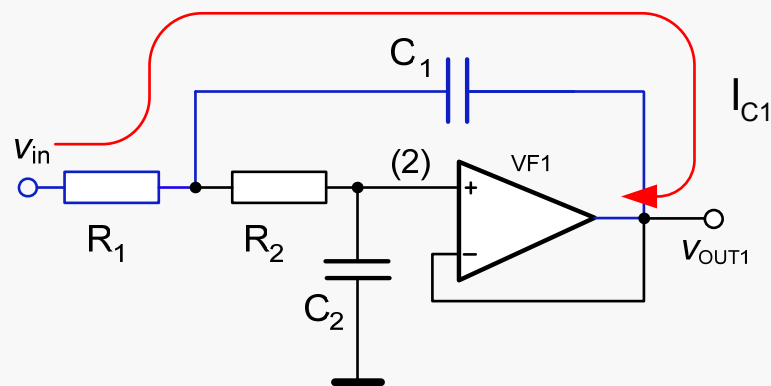Effect of parasitic zeros in the AC response of frequency filter

[*] Geffe, P. R., IEEE Trans., Vol. CAS-23, pp.45-55, 1976
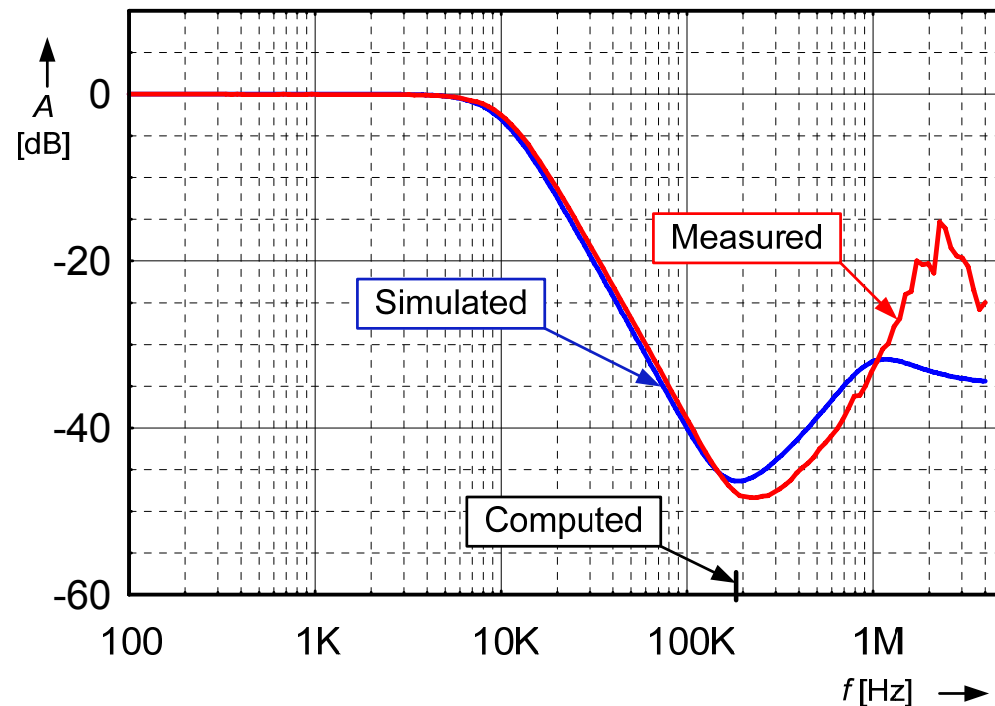[**] Schmid, H. Moschytz, G.S, Circuits and Systems, vol.1, 1998, p. 57-60.

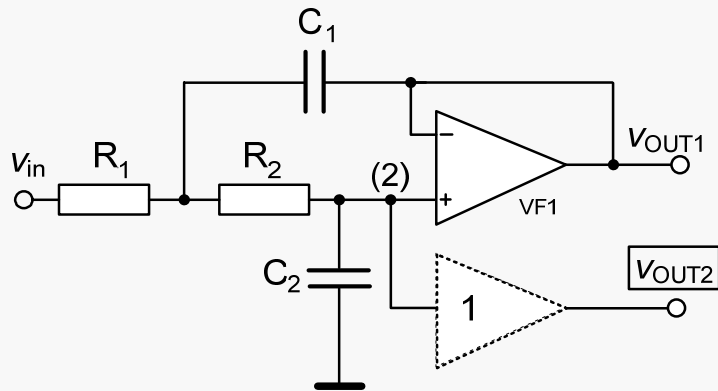# Example: real Sallen-Key filter

LP Sallen-Key biquad [*]

parasitic transfer zeros in the stopband

Parasitic zero occurs at :

$$f_Z = \frac{1}{2\pi} \sqrt[3]{\frac{2\pi GBW}{R_0 R_2 C_1 C_2}}$$

[*] Sallen.R.P-Key.E.I., Circuit Theory. Vol. 7. 1955

Real Sallen-Key: compensation

Improved Type II Sallen-Key
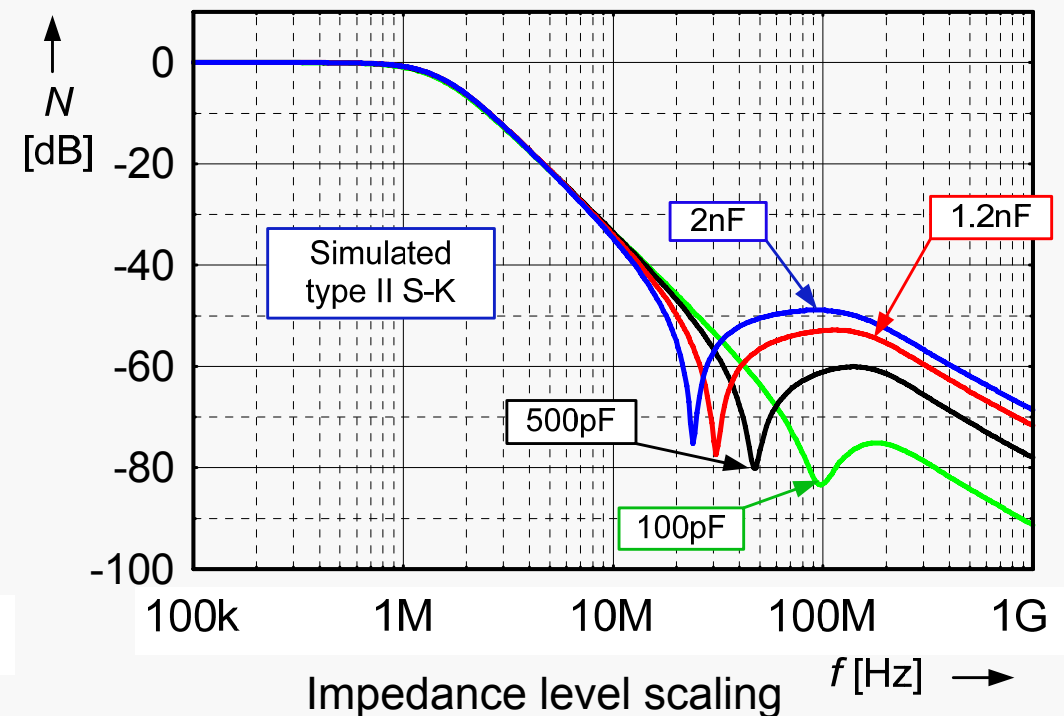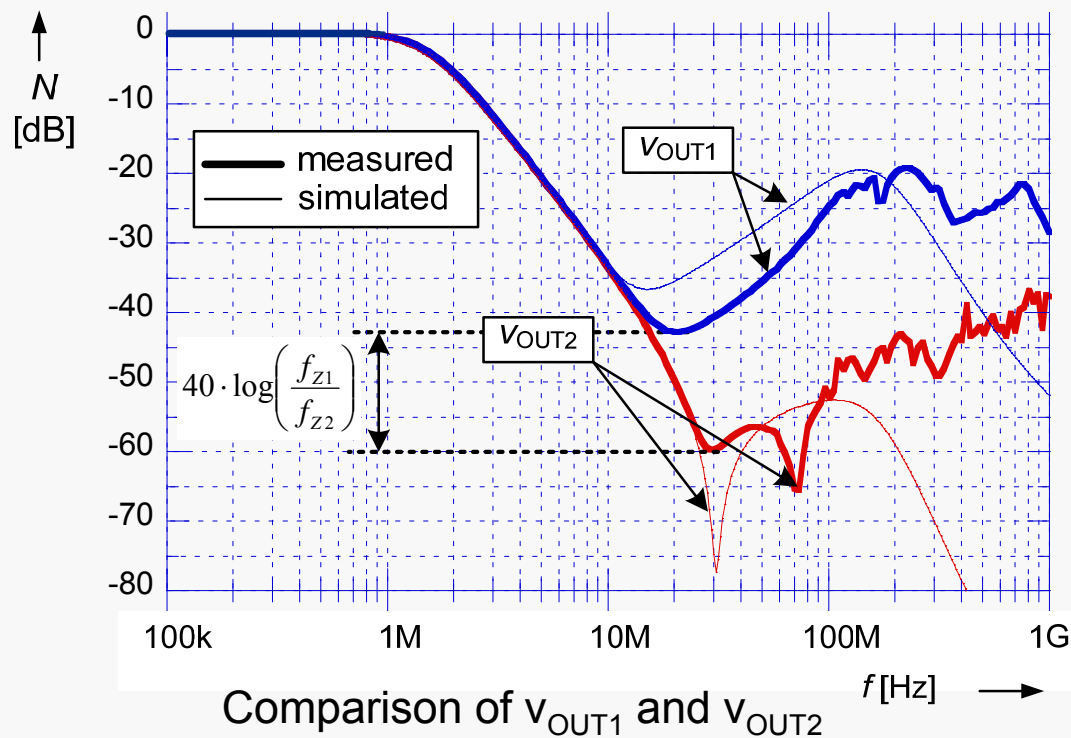
$$f_{Z(2)} \cong \frac{1}{2\pi} \sqrt{\frac{A \cdot \omega_P}{C_1 R_{OUT}}}$$

reduced order of the root, only R_{out} and C_1 contribute to the frequency ➔ **Higher attenuation**

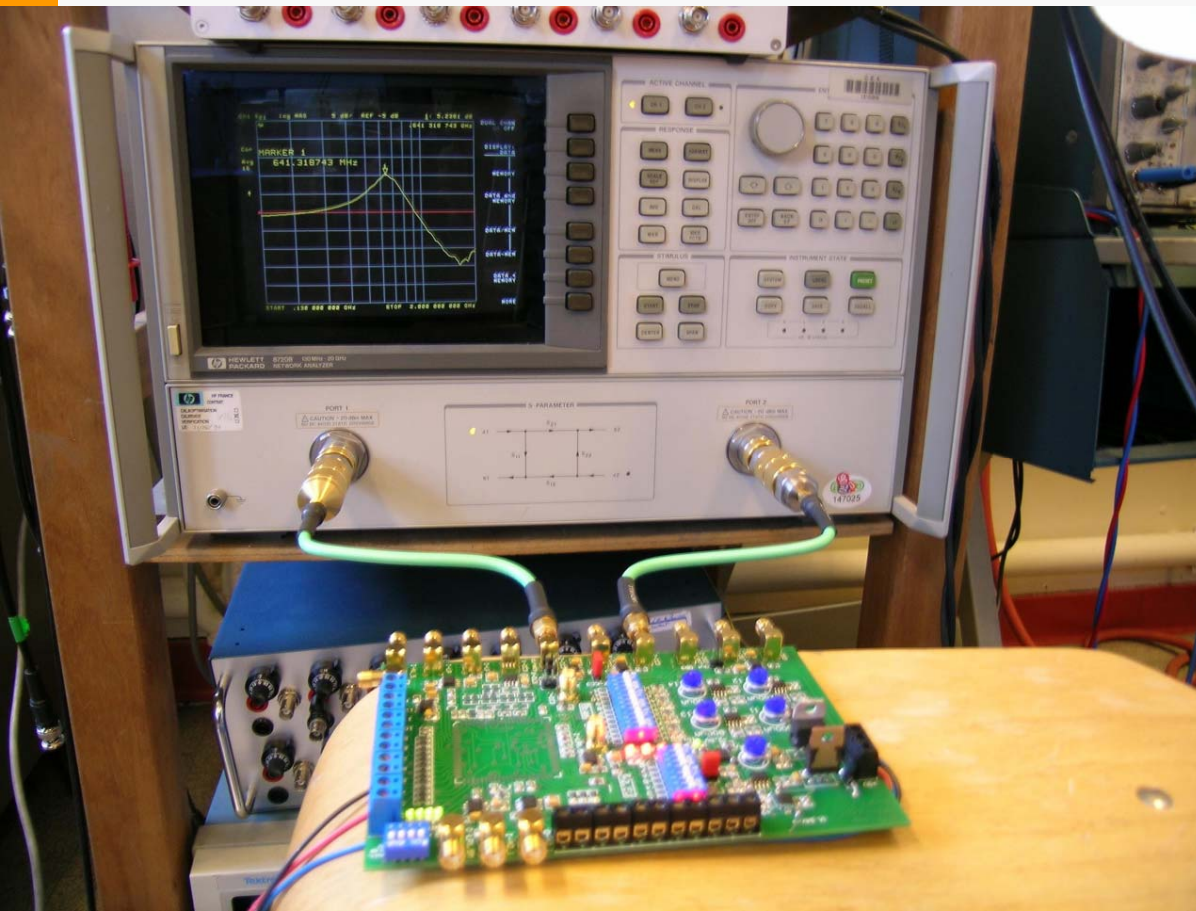Comparison of v_{OUT1} and v_{OUT2}

Impedance level scaling

III.1
CCII biquadratic section

Proposed solution

Removal of the parasitic zeros ensures constant -40dB roll-off

➔ Division of the frequency band in two regions:

- **Region up to f_0,** where the DC transfer and resonance gain are ensured by the active element

- **Stop-band region**, where the high attenuation is ensured by the passive RC filter

➔ **Design rules:** Interruption of direct signal way,
Passive filters containing grounded capacitors

Adopted solution: topological transformation of circuits presented in [*]

[*] Liu, S-I., Tsao,H-W; Wu,J., Tsay, J-H. "*Realizations of the single CCII biquads with high input impedance"*, IEEE Symposium on Circuits and Systems, 1991.
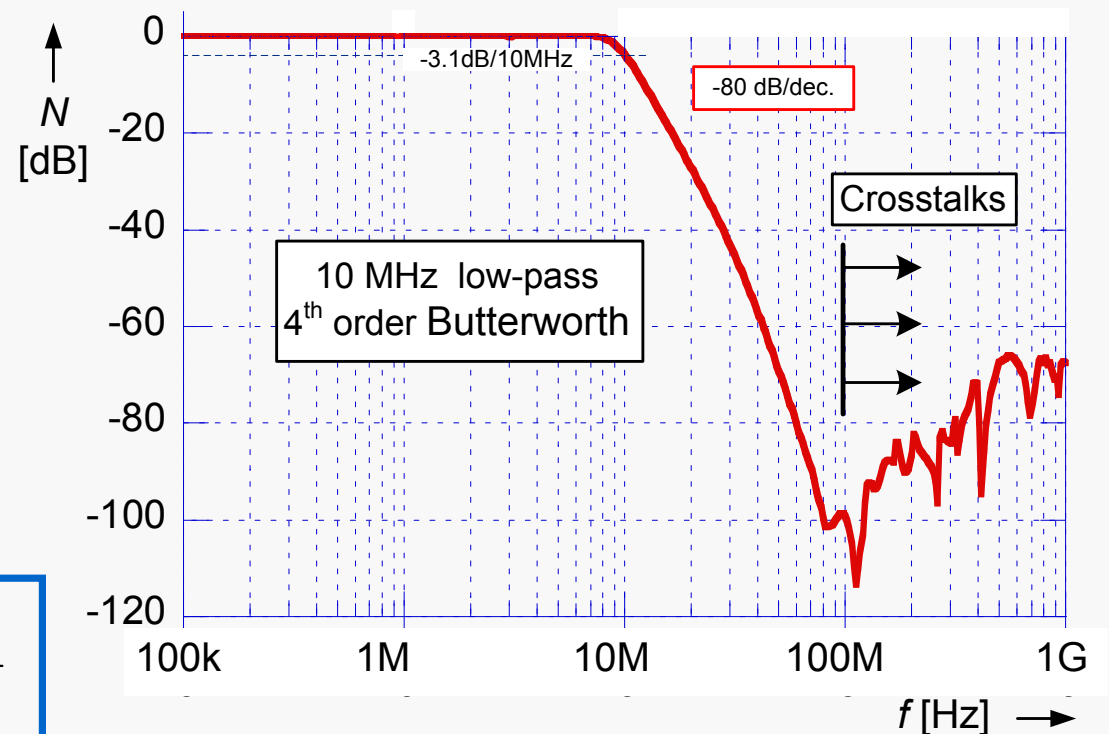
New biquadratic section CCII-
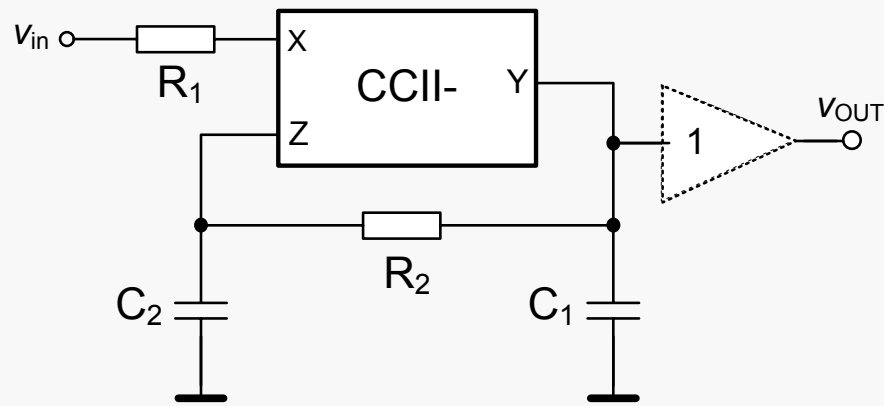
CCII- low-pass biquadratic section with eliminated parasitic transfer zero

$$f_0 = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \qquad Q = \frac{\sqrt{R_2}}{\sqrt{R_1}}\cdot\frac{\sqrt{C_1 C_2}}{C_1 + C_2} = \frac{1}{2}\cdot\sqrt{\frac{R_2}{R_1}}\bigg|_{C1=C2}$$

Stop band behavior (single pole model of CCII):

$$H(s) = \frac{\Omega_0^2}{\left(s^2 + s\cdot\Omega_0\big/Q_0 + \Omega_0^2\right)}\cdot\frac{\left(\omega_P\cdot A_0 + s\right)}{\left(\omega_P\cdot(1+\alpha)\cdot A_0 + s\right)}$$

measured AC response of 10MHz 4th order LP filter

Summary of achieved features

F_0: 1.5M 5M 10M 20M 50M

N [dB]

2nd cascade
FDNR LP

100k 1M 10M 100M 500M

f [Hz]
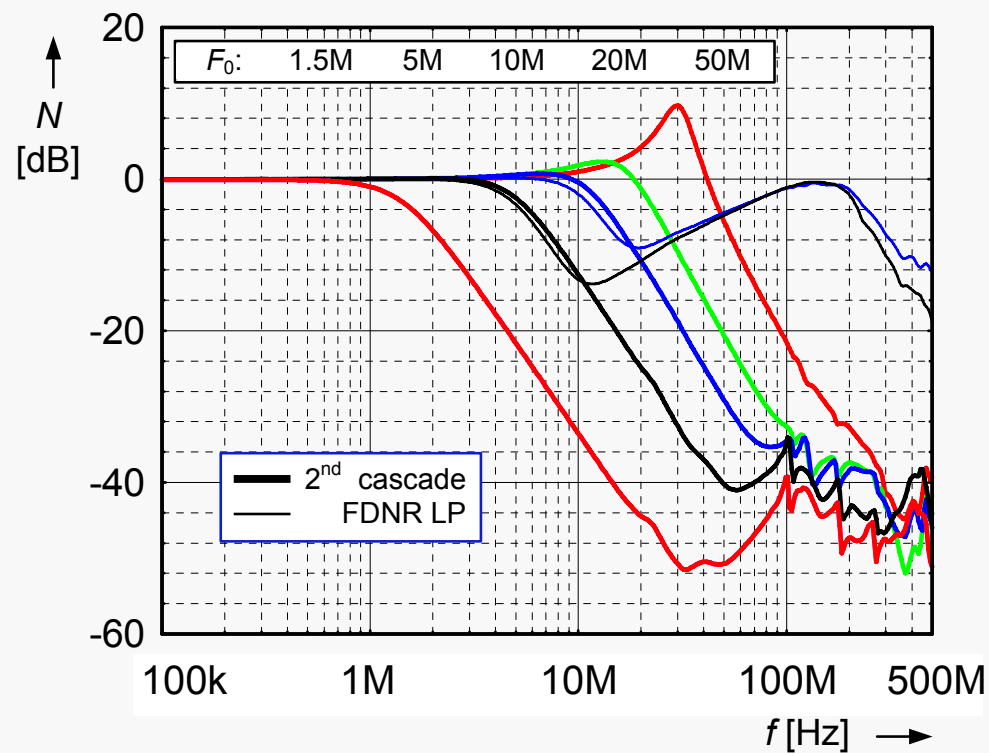
Attenuation floor independent of the f_0.
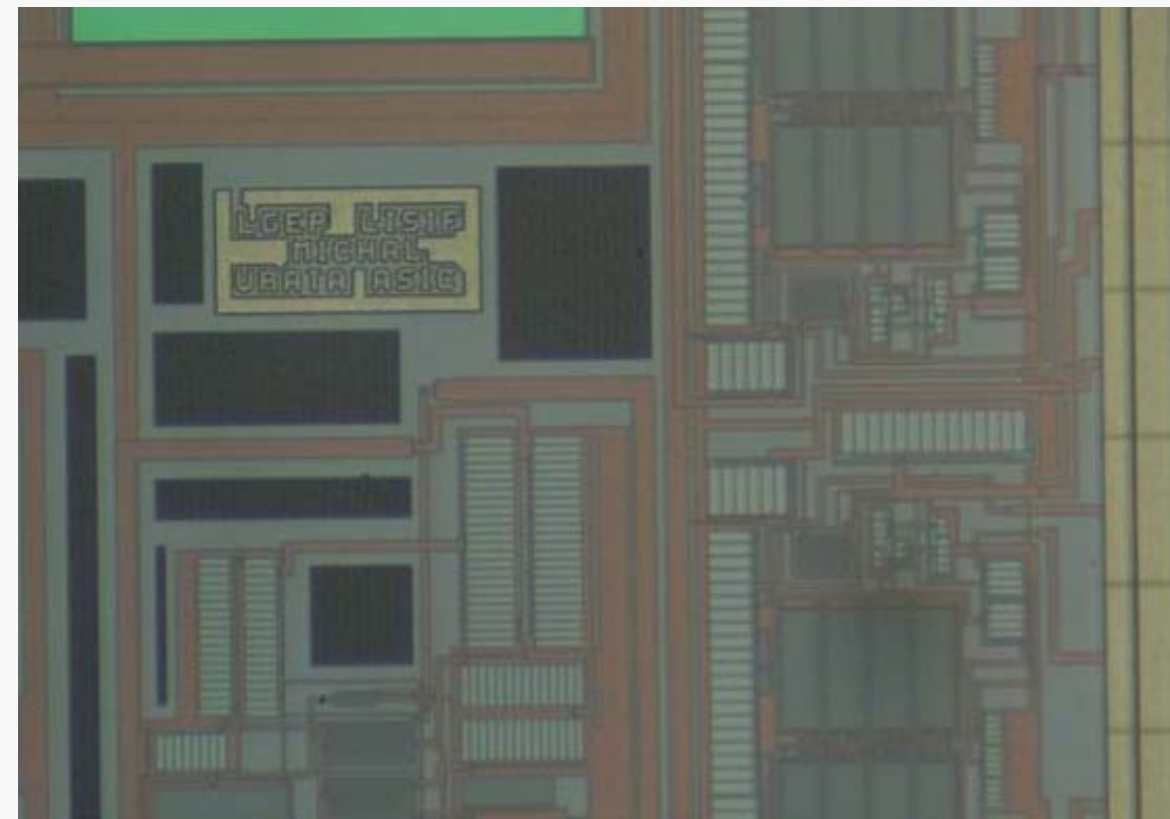comparison with lossy R-FDNR biquad [*]

- **The attenuation is only limited by signal leakage**

- **Does not depend on the f_0**

- **Using low-performance voltage buffer is allowed**

- **Direct connection to the DAC input**

➔ **price and power consumption are reduced**
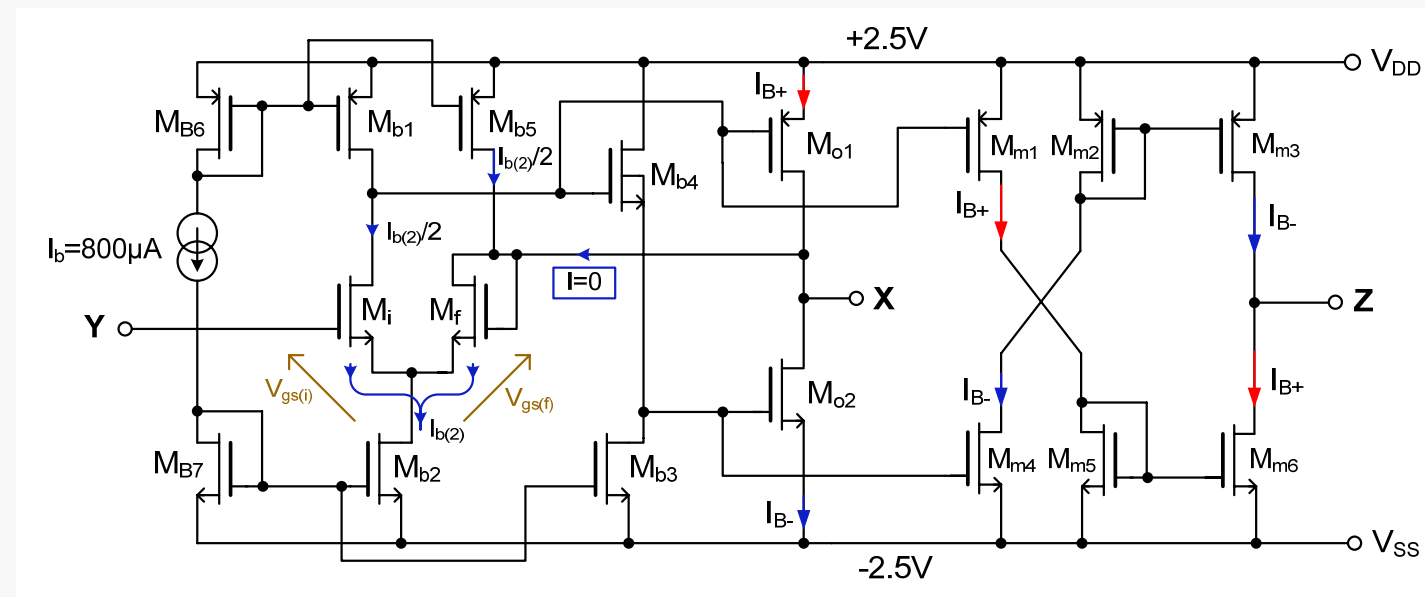
[*] Martinek, P. Radioelek, 2006

III.2
High performance
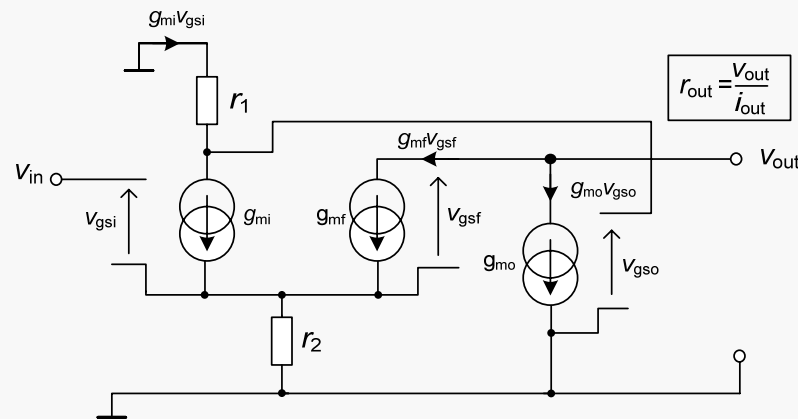# CCII current conveyor

Design of ultra-low R_{out} CCII-

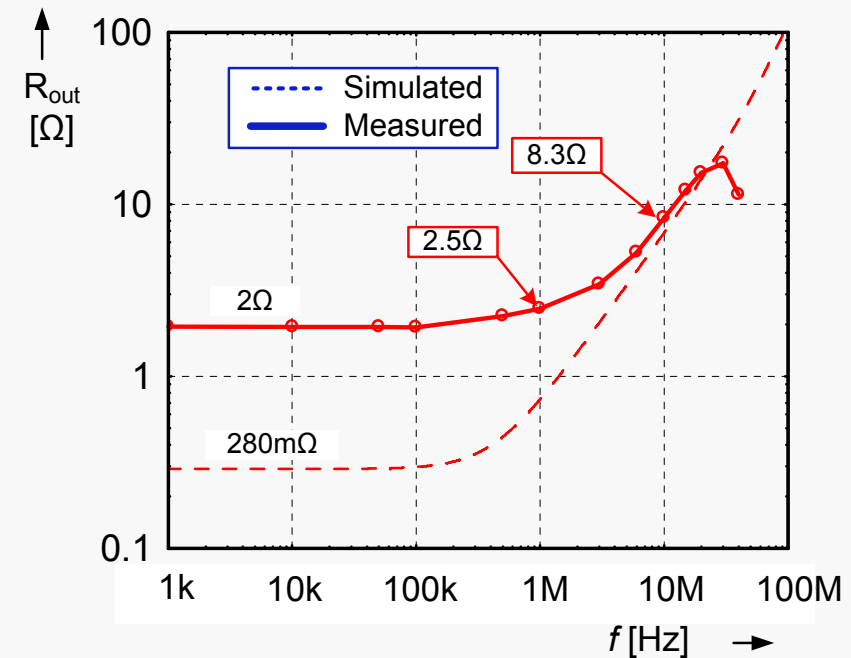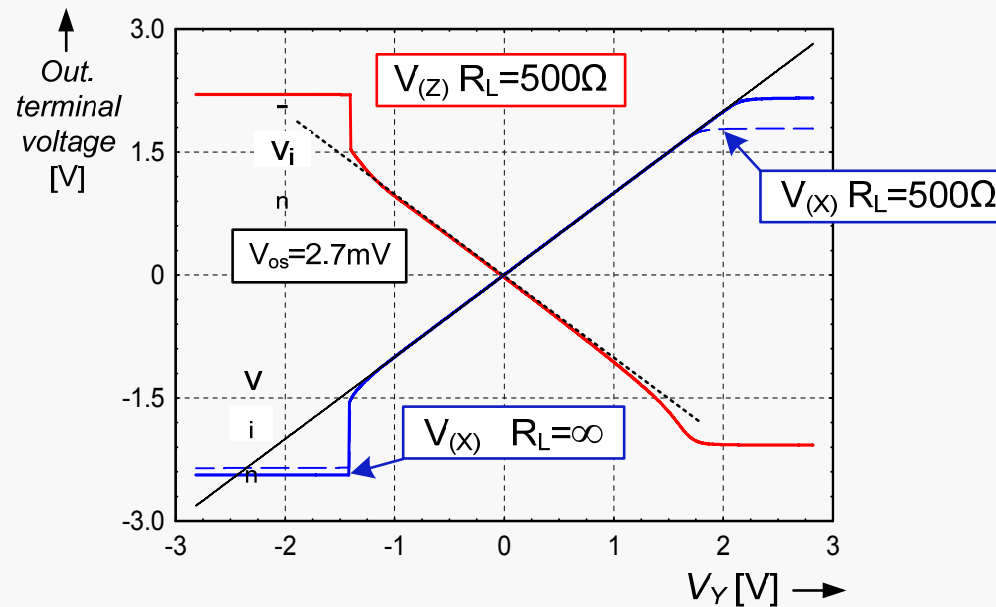CCII- with very low output resistance voltage buffer

simplified small signal model

$$r_{out} = \frac{v_{out}}{i_{out}} = \frac{2 \cdot r_2 + 1}{r_2 \cdot g_{mf} + r_1 \cdot r_2 \cdot g_{mo} \cdot g_m + g_m}$$

$$\approx \frac{2}{r_1 \cdot g_{mo} \cdot g_m} \Rightarrow 0$$

Hassan O. et al, Circuit and Systems II, Vol. 49 (2002)

Performances: state-of-the-art

V_{DD}	+/- 2.5V
Quiescence current	11 mA
Port X,Z voltage swing	+/- 1.5 V
Port X,Z driving capacity	+/- 20 mA
Port Z DC impedance	~7.5 MΩ
Port X offset voltage	2.7 mV
Port Z offset current	2.25 µA
-3dB AC transfer Y→X	~110 MHz

Summary of achieved performances

Recently published results on UVC [*]:

terminal	10kHz	1MHz	10MHz
z+	2.1Ω	10Ω	89Ω
z-	0.9Ω	8.2Ω	76kΩ

[*] Minarcik,M., Vrba,K. ICN'07

Experimental result: 1.5MHz LPF
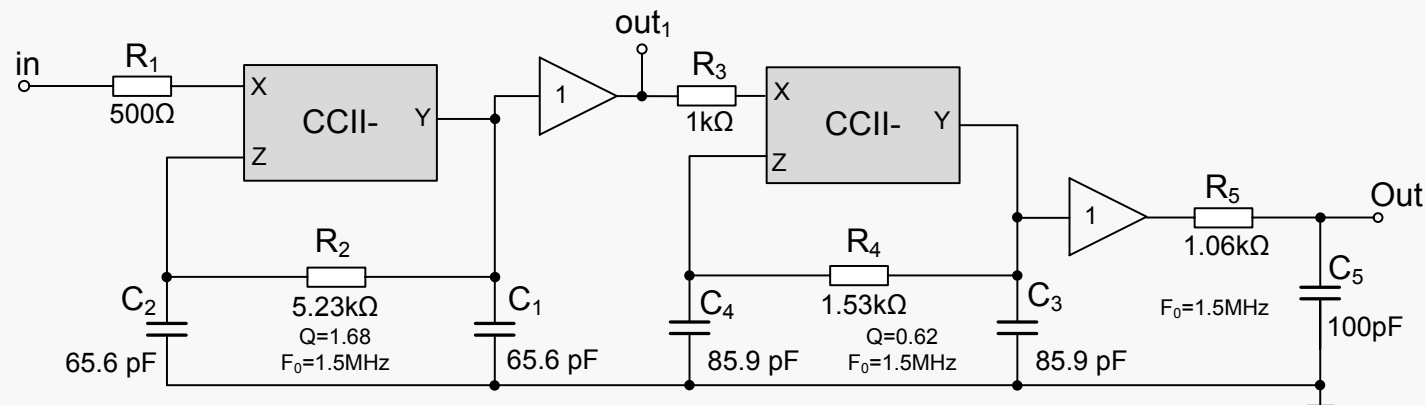
5th order LP filter (Butterworth) using new CCII biquadratic sections

Characteristic of
1.5 MHz 5th order LP filter ⟹

IV.
Summary

Summary: example of test facility

Conclusion: scientific contribution

New generation of differential (instrumentation) amplifiers
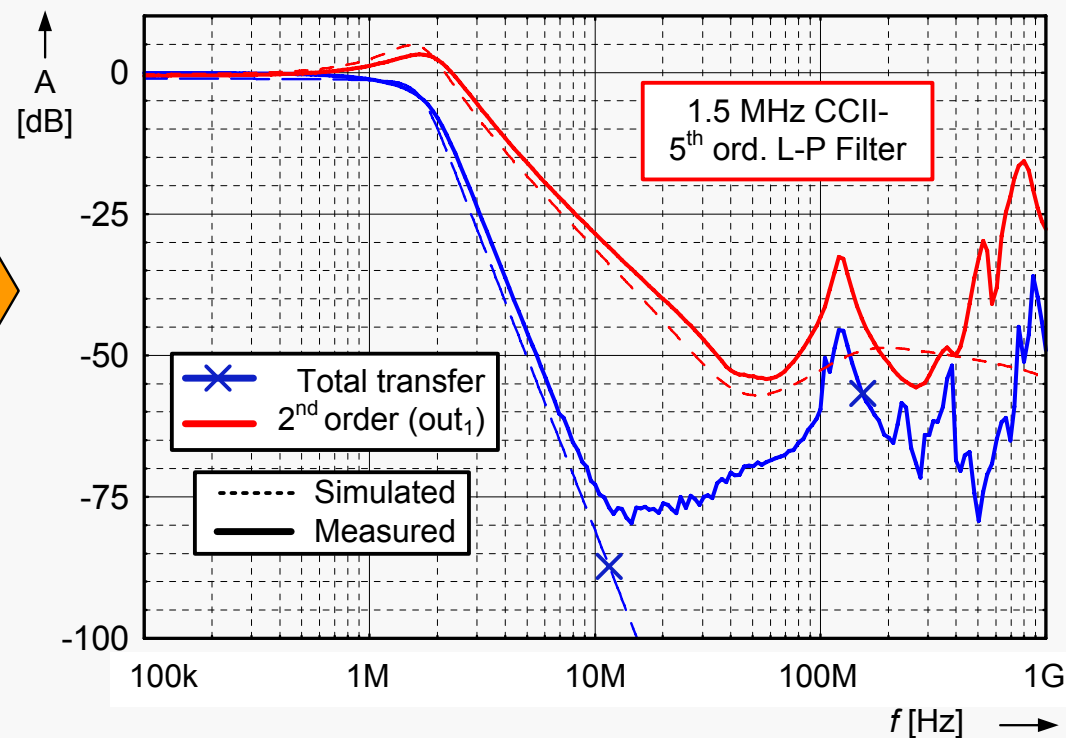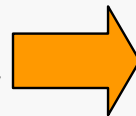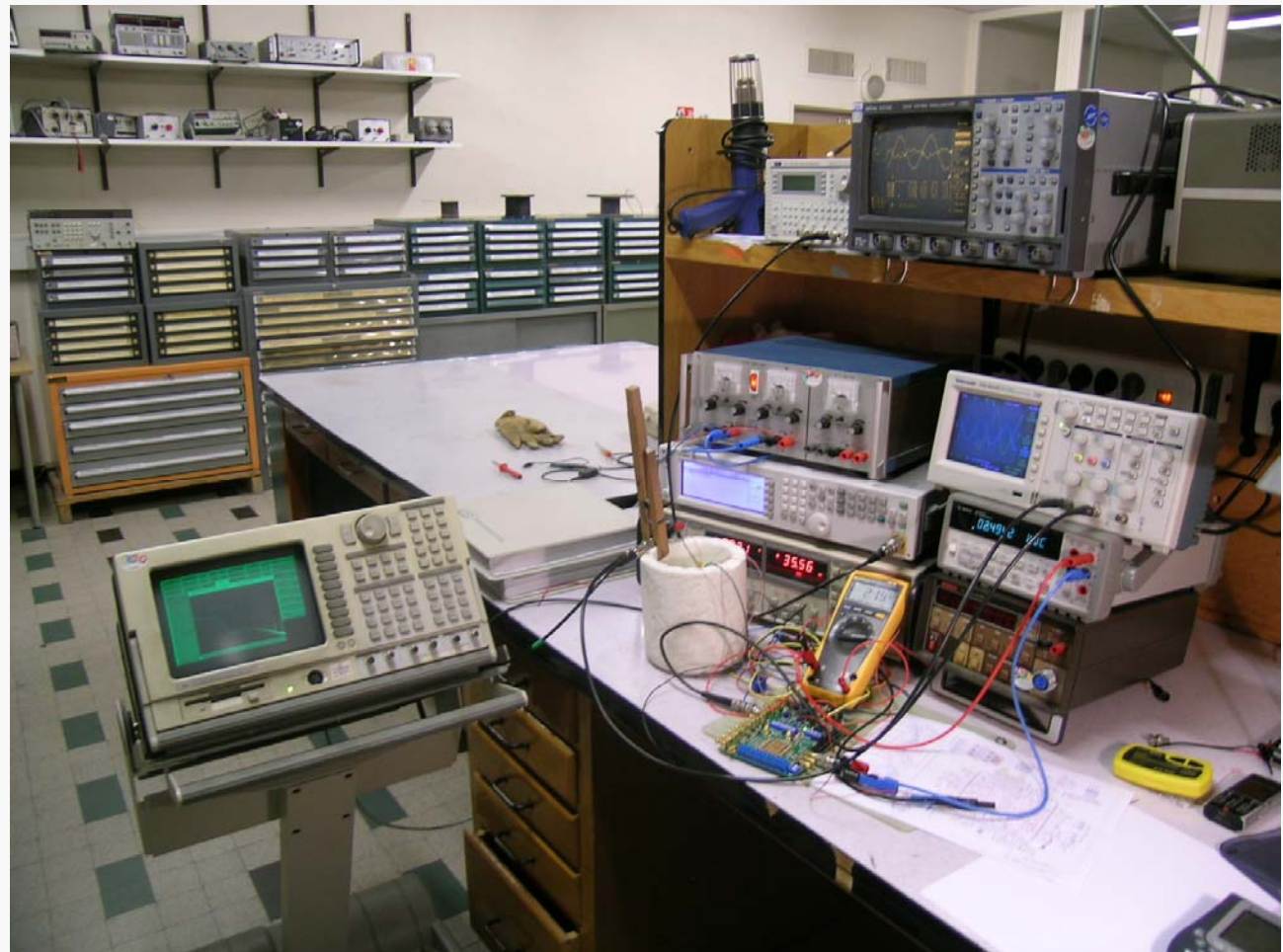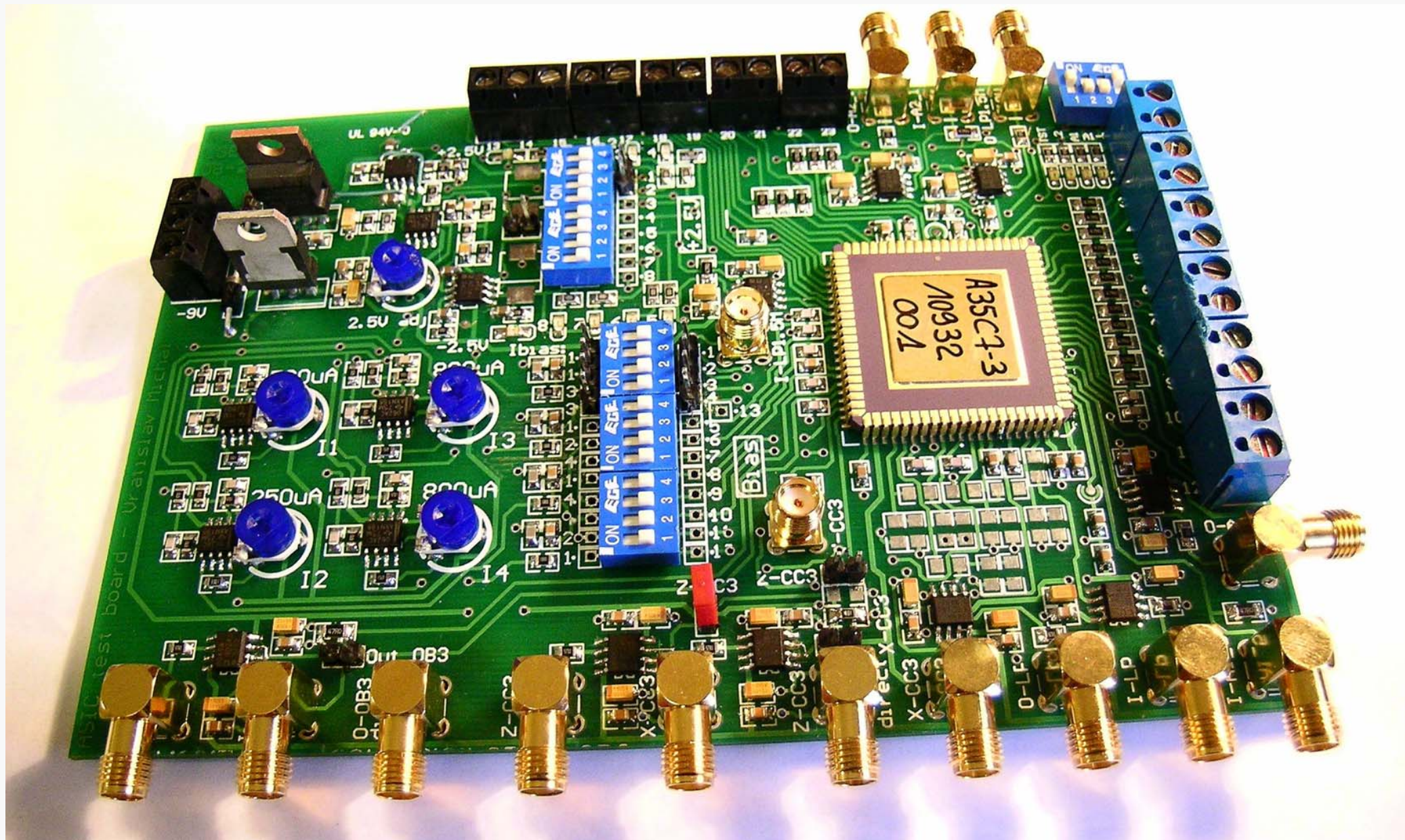
Feedback-free architecture. State-of-the-art of the performances, competitive with the bipolar technology: high BW, low power consumption, low noise level

Comparison:

	Type I	Type II	AD8045 (OA)	LT1226 (OA) 25dB stable	INA103 (IA)
Iq	2.1 mA	1.3 mA	19 × 3mA	7 × 3mA	9mA
− 3dB BW (290K)	(GBW=1GHz)	4 MHz	1GHz	1000	0.08
− 3dB BW (77K)	(GBW=1.7GHz)	10 MHz	-	-	-
Noise (290 K)	5 nV/Hz$^{1/2}$	5 nV/Hz$^{1/2}$	3 nV/Hz$^{1/2}$	2,6	1
Noise (290 K)	2 nV/Hz$^{1/2}$	3 nV/Hz$^{1/2}$	-	-	-

Cryogenic instrumentation, innovative design approaches

Analytical thermal model of the MOS, hybrid voltage-current biasing method

Analog front-end circuits optimization

New structures with improved behavior in stop-band, large extension of bandwidth

Fabricated circuits ready to be used in the new generation THz detector test set-up

Perspectives: Integration of the electronics in the THz test-bench

Implementation of designed circuits in industrial applications

Shrnutí doktorské práce

Vývoj nové generace rozdílových zesilovačů pro měřící účely

Struktura v otevřené smyčce ZV, parametry plně porovnatelné s konkurencí i s bipolarnim zesilovači: velká šířka pásma, velmi nízká spotřeba a úroveň šumu

Porovnání:

	Type I	Type II	AD8045 (OA)	LT1226 (OA) 25dB stable	INA103 (IA)
Iq	**2.1 mA**	**1.3 mA**	19 × 3mA	7 × 3mA	9mA
− 3dB BW (290K)	**(GBW=1GHZ)**	**4 MHz**	1GHz	1000	0.08
− 3dB BW (77K)	**(GBW=1.7GHZ)**	**10 MHz**	-	-	-
Noise (290 K)	**5 nV/Hz$^{1/2}$**	**5 nV/Hz$^{1/2}$**	3 nV/Hz$^{1/2}$	2,6	1
Noise (290 K)	**2 nV/Hz$^{1/2}$**	**3 nV/Hz$^{1/2}$**	-	-	-

Obvody pro velmi nízké teploty: nový přístup k návrhu

Analytický model transistoru MOS, hybridní polarisace napětí-proud

Obvody analogového předzpracování signálu

Obvody biquadratických filtrů s vylepšeným potlačení v nepropustném pásmu. Zvýšení maximálího mezního kmitočtu a snížení odběru

Integrované Obvody CMOS byly vyrobeny a jsou připraveny k použití v měřící soustavě pro bolometrické detektory THz

Perspektiva: Integrace zesilovačů v měřící soustavě, optimalizace

Implemenace principů a metod návrhu v návazných průmyslových aplikacích

Contribution scientifique

Nouvelle génération d'amplificateurs différentiels d'instrumentation

Architecture en boucle ouverte, niveau de l'état de l'art. Compétitive avec des technologies bipolaires: grande BP, consommation réduite, bas bruit

Comparison:

	Type I	Type II	AD8045 (OA)	LT1226 (OA) 25dB stable	INA103 (IA)
Iq	2.1 mA	1.3 mA	19 × 3mA	7 × 3mA	9mA
– 3dB BW (290K)	(GBW=1GHZ)	4 MHz	1GHz	1000	0.08
– 3dB BW (77K)	(GBW=1.7GHZ)	10 MHz	-	-	-
Noise (290 K)	5 nV/Hz$^{1/2}$	5 nV/Hz$^{1/2}$	3 nV/Hz$^{1/2}$	2,6	1
Noise (290 K)	2 nV/Hz$^{1/2}$	3 nV/Hz$^{1/2}$	-	-	-

Instrumentation cryogénique: approche de conception innovante

Modèle analytique de transistor MOS, polarisation hybride tension-courant

Circuiterie d'entrée analogique optimisée

Structures de filtres biquadratiques avec un comportement "hors-bande" amélioré, élargissement considérable de la bande-passante
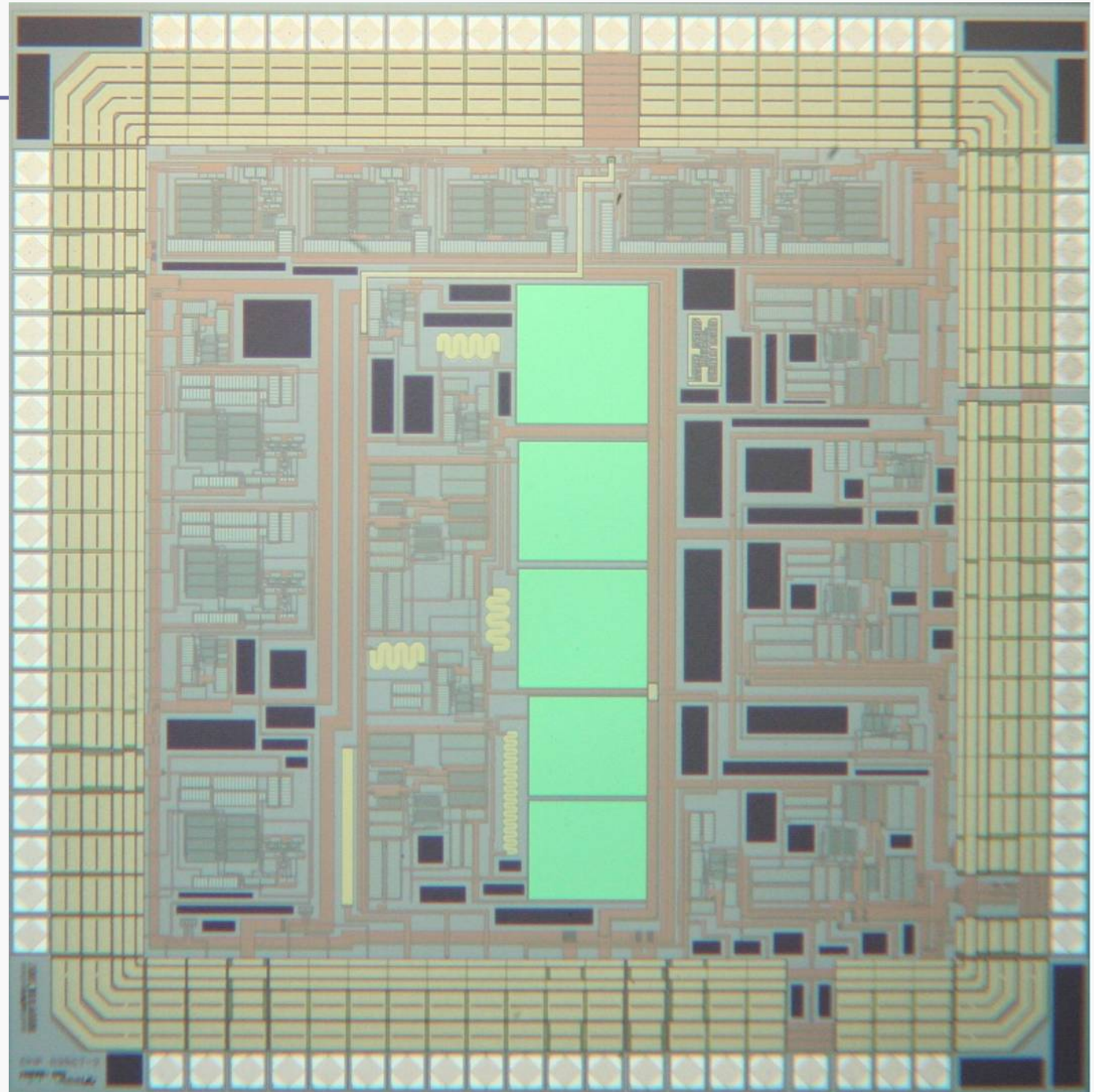
Circuits fabriqués, prêts à être utilisés en instrumentation THz

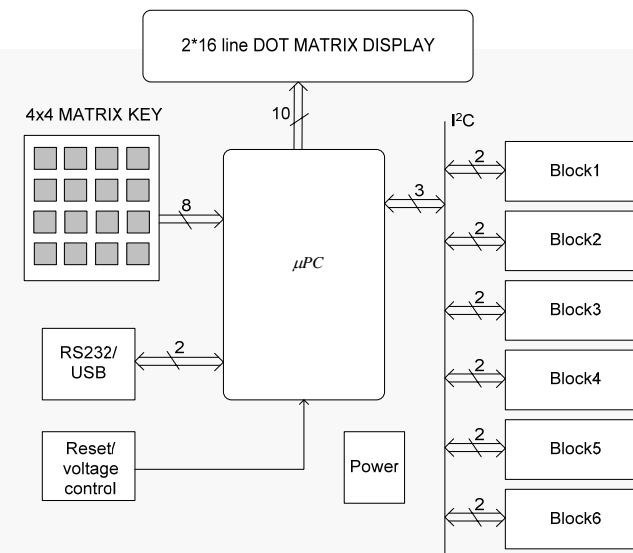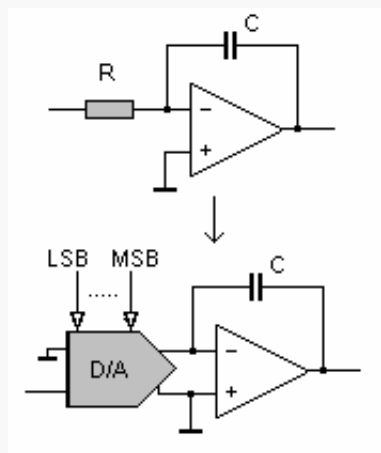**Perspectives: Intégration des circuits en question dans un banc de test**

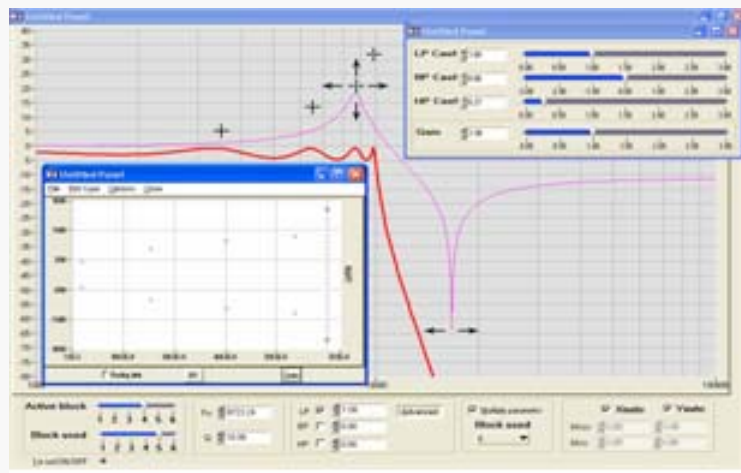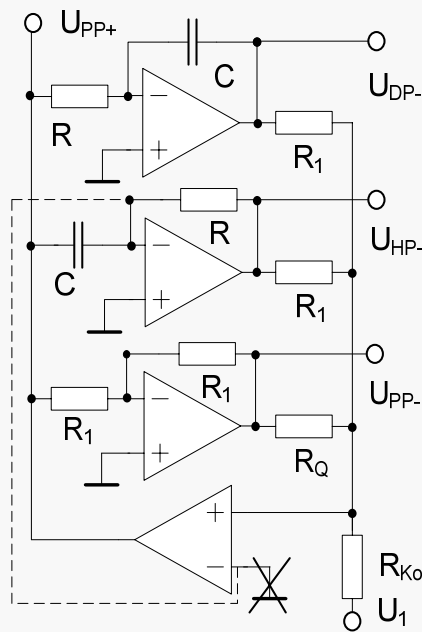Mise en œuvre des circuits dans des applications industrielles
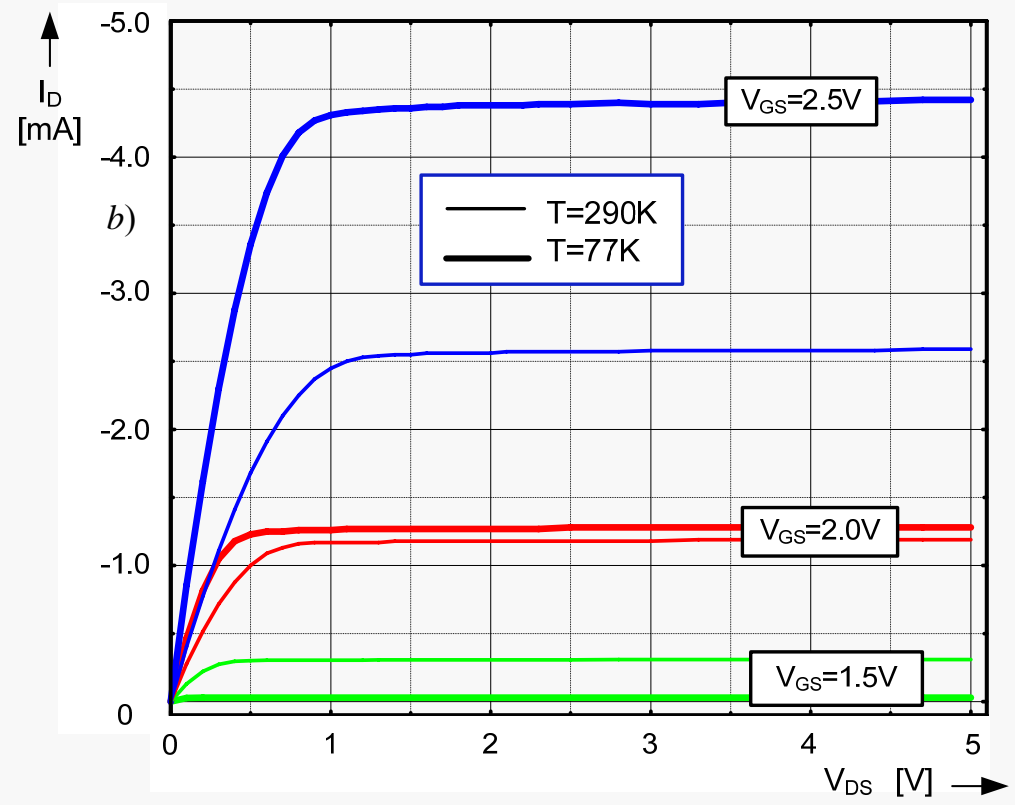
Thank you

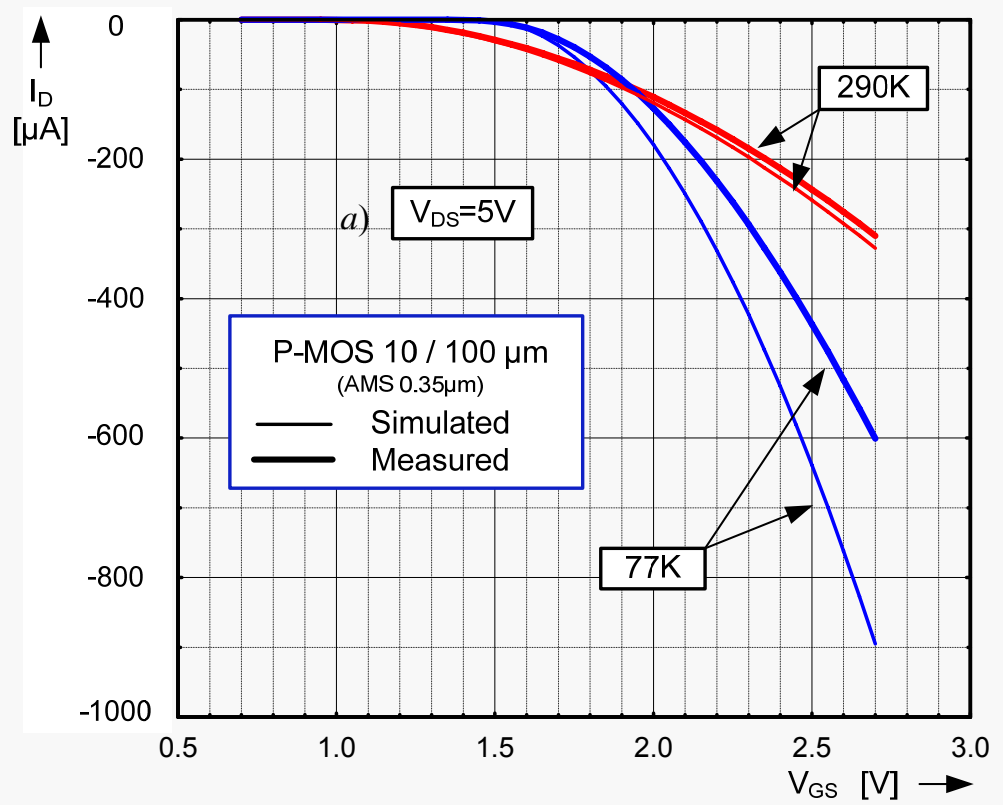# Supplementary slides

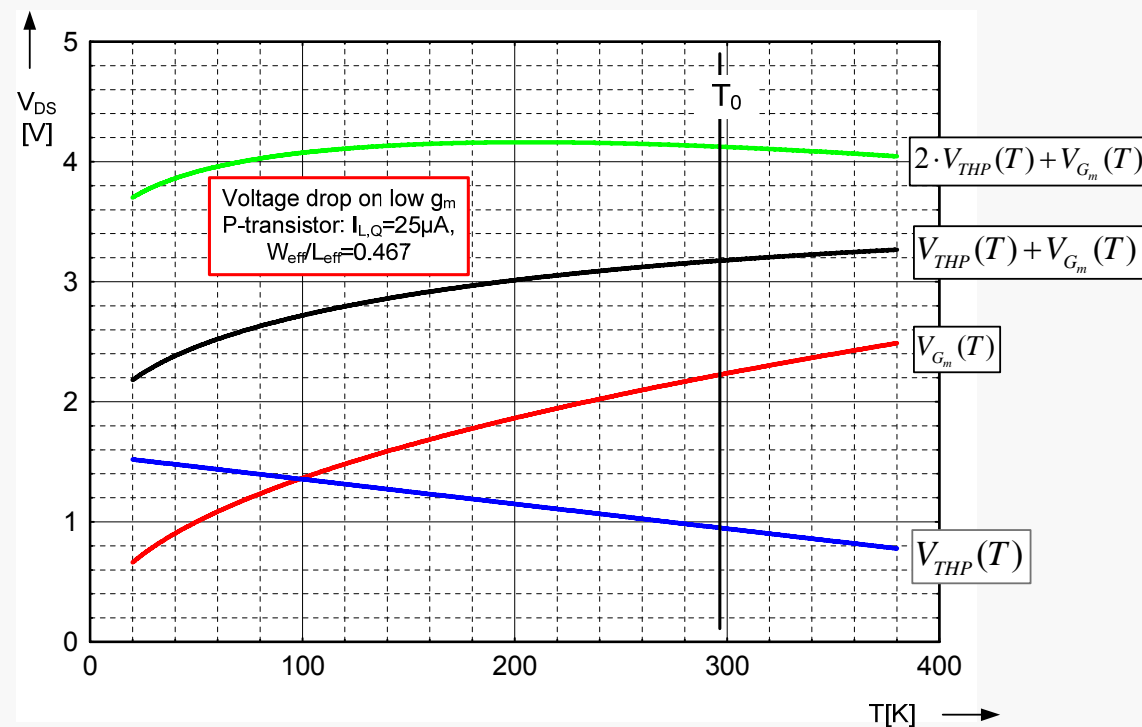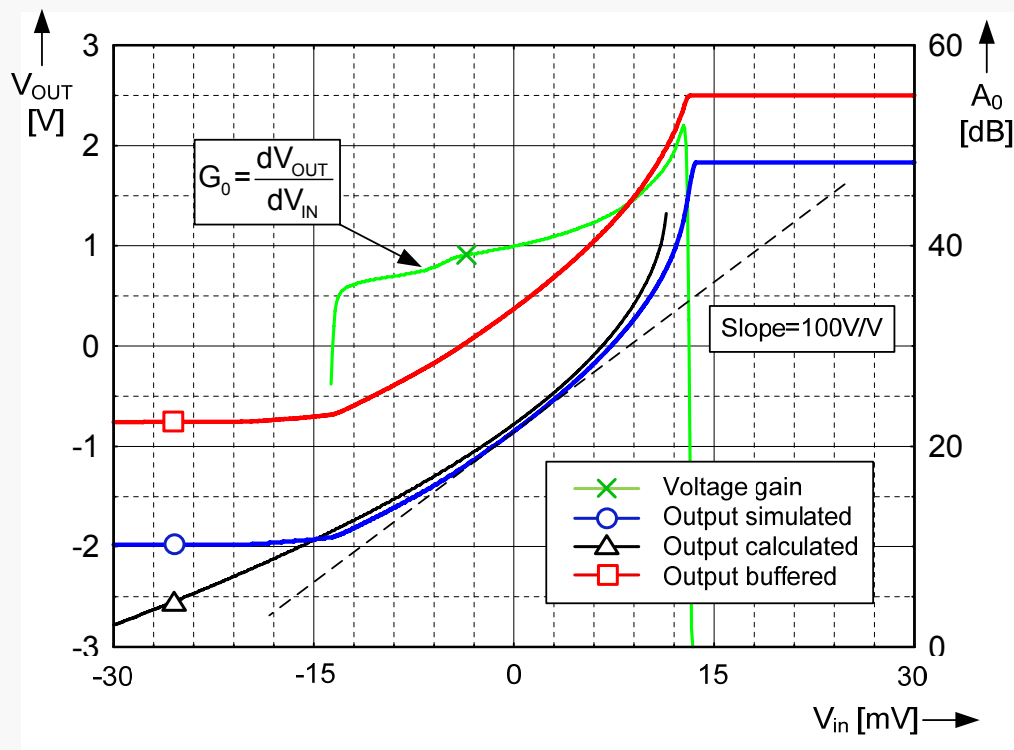# Concurrence to DSP: YES[*]

[*] V. Michal et al. "*The analog Filter Design and Interactive Analog signal Processing by PC*" WSEAS (2005)

Accuracy of BSIM-3

Comparison of characteristic obtained by measurements and simulations on a PMOS transistor
W/L=10µm / 100 µm

DC characteristic, bias point

Simulated and calculated DC transfer characteristics
(V$_{DD}$ = 5 V)

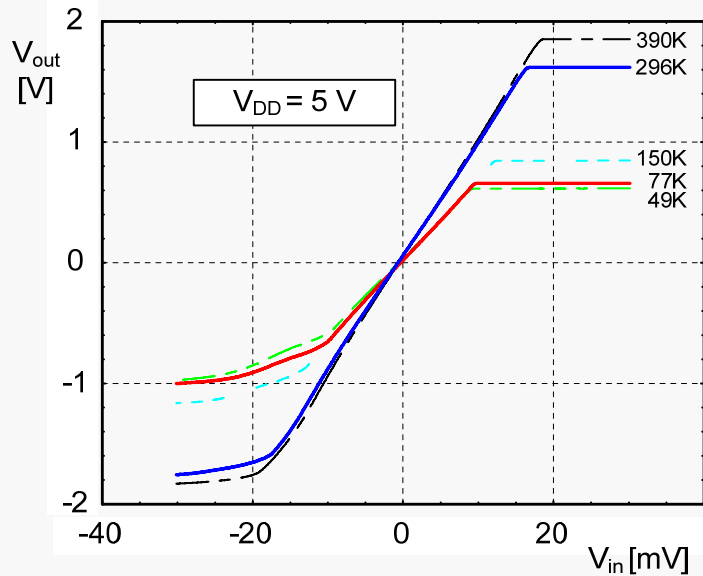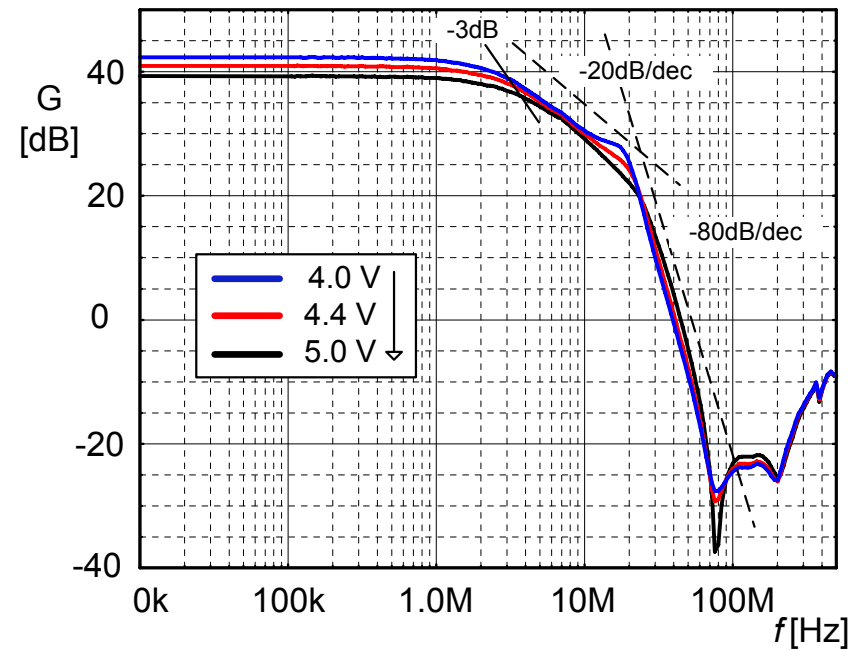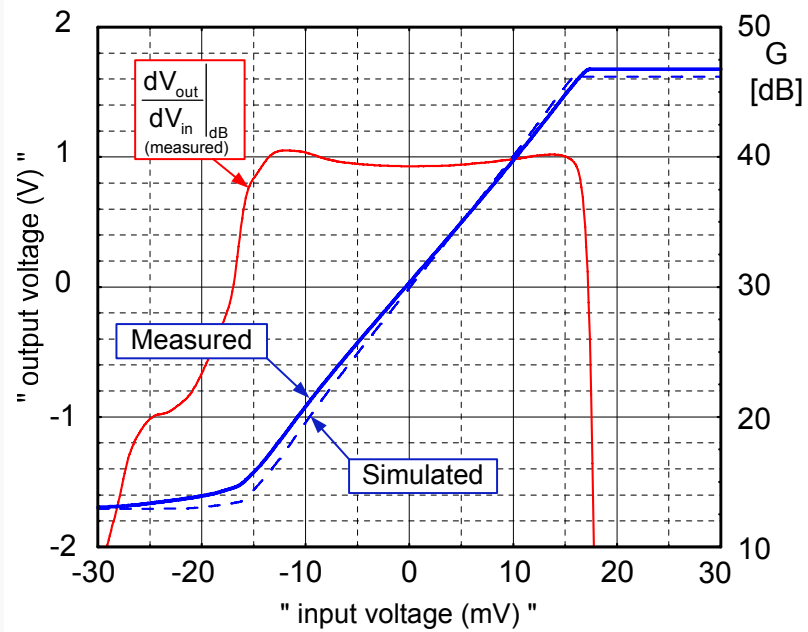*Temperature evolution of DC output voltage*

Diff. pair size

$$\frac{W_D}{L_D} = 8 \cdot \frac{W_{eff}}{L_{eff}} \cdot \frac{I_{L,Q}}{I_B} \cdot G_0^2$$

$$V_{OUT} = V_{DD} - \underbrace{|V_{THP}| \cdot \left[1 + \alpha_{THX} \cdot (T - T_0)\right]}_{V_{THP}(T)} - \underbrace{\sqrt{\frac{2 \cdot I_{D1}}{KP_P \left(T/T_0\right)^{-x} W_{eff}/L_{eff}}}}_{V_{Gm}(T)}$$

Results: wide temperature measurements
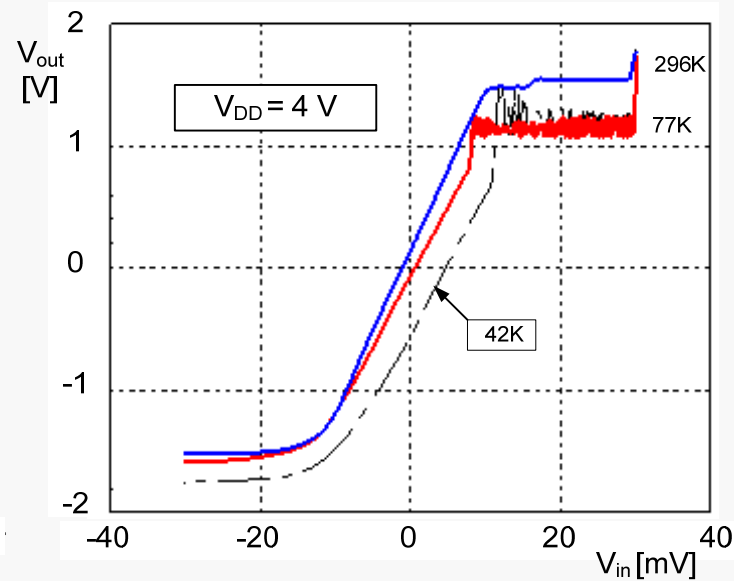
Comparison with industrial state of the art

Key parameters of developed amplifiers

MEASURED PARAMETERS	TYPE *I* AMPLIFIER	TYPE *II* AMPLIFIER
Operating supply voltage	4.1 V to 5.5 V	3.6 V to 5.5 V
Quiescent current	2.1 mA	1.3 mA[1]
− 3 dB bandwidth (T = 290 K)	10 MHz (GBW=1GHZ)	4 MHz at V_{DD} = 5 V
− 3 dB bandwidth (T = 77 K)	17 MHz (GBW=1.7GHZ)	10 MHz at V_{DD} = 5 V
Input noise (T = 290 K)	5 nV/Hz$^{1/2}$	5 nV/Hz$^{1/2}$
Input noise (T = 77 K)	2 nV/Hz$^{1/2}$	3 nV/Hz$^{1/2}$
Gain G_0 (T = 290 K)	39.85 dB	39.3 dB at V_{DD} = 5 V
Δ Gain 270 K − 390 K	− 0.12 dB	− 0.5 dB at V_{DD} = 4 V
Gain error (at T = 77 K)	− 1.2 dB	− 1.3 dB at V_{DD} = 4 V
THD[2] (V_{out} = 0.3 V_{pp})	1 %	0.03 %
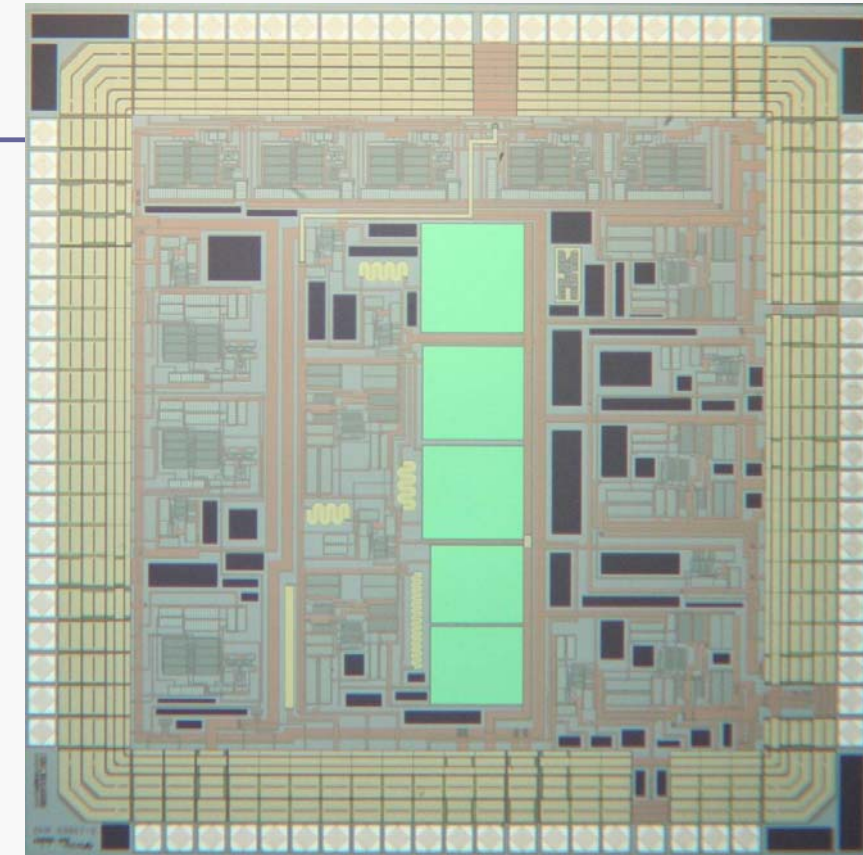
Industrial differential amplifiers (room temperature)

Type	Configuration	GBW [MHz]	SR [µV/s]	VDD [V]	Iq [mA]	Input noise nV/√Hz	Other
AD8045	OA Bipolar	1000	1350	3.3 - 12	19 × 3	3	
LTC6401-20	Fixed gain 20dB+/-0,6dB Bipolar	1300	4500	2,85-3,5	50 × 3	2,1	R_{in}=200Ω
LT1226	OA Bipolar	1000	400	5-36	7 × 3	2,6	25dB stable
OPA699	OA Bipolar	1000	1400	5-12	22,5 × 3	4,1	12dB stable
OPA2354	OA CMOS	250	150	2,7-5,5	7,5 × 3	6,5	
INA2331	Instrumentation CMOS	50	5	2,5-5,5	0,5	46	
INA103	Instrumentation BIPOALR	80	15	9-25	9	1	

Global performances: state of the art
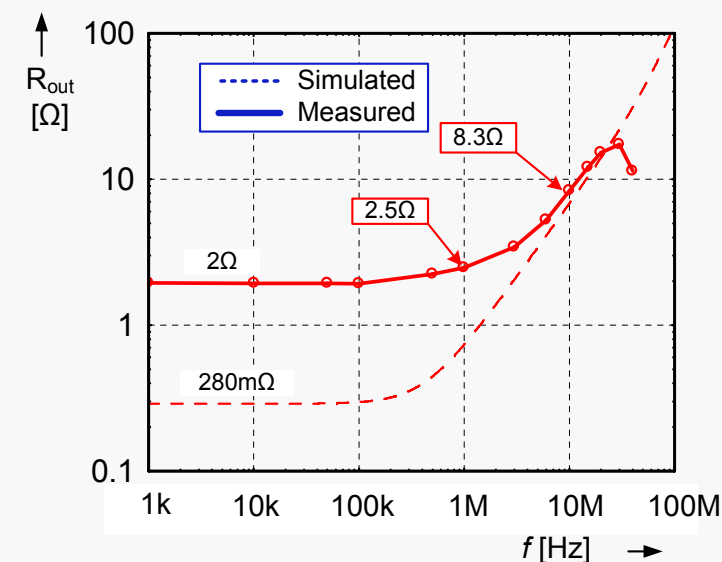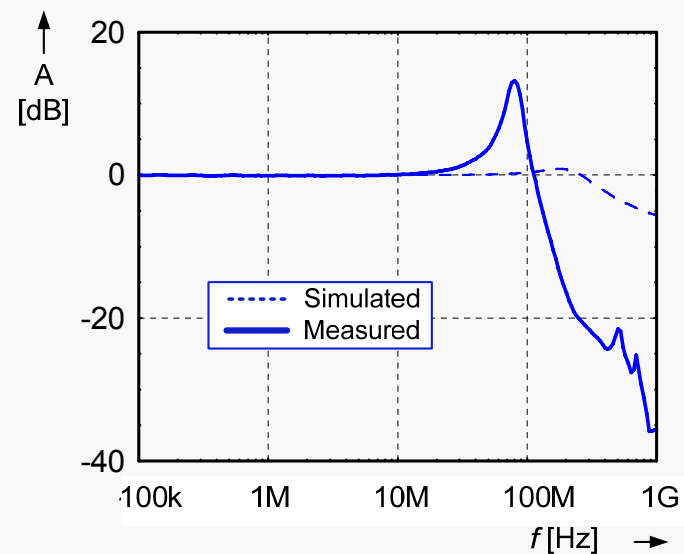
*measured and simulated resistance of output terminal **X***

measured and simulated AC response of the unity gain voltage buffer

V_{DD}	+/- 2.5V
Quiescence current	11 mA
Port X,Z voltage swing	+/- 1.5 V
Port X,Z driving capacity	+/- 20 mA
Port Z DC impedance	~7.5 MΩ
Port X offset voltage	2.7 mV
Port Z offset current	2.25 µA
-3dB AC transfer Y→X	~110 MHz
Port X resistance @ DC	2 Ω
Port X impedance @ 1MHz	2.5 Ω
Port X impedance @ 10MHz	8.5 Ω

Summary of achieved performances

Recently published results on UVC [*]:

terminal	10kHz	1MHz	10kHz
z+	2.1Ω	10Ω	89Ω
z-	0.9Ω	8.2Ω	76kΩ

[*] Minarcik,M., Vrba,K. "*Continuous-Time Multifunctional Filters with Wide Bandwidth Using Universal Voltage Conveyors* " IEEE International Conference on Networking (ICN'07)

AC & DC characteristics, sensitivity

ΔG=0.4dB in the range of: -3dB
T <-60º;100º>C

-40dB/dec

ΔT=30ºC
T

0ºC

SPICE level-7
model

G [dB]

100k   1M   10M   100M

F [Hz]

$G_0 = \dfrac{dV_{OUT}}{dV_{IN}}$

Slope=100V/V

	Voltage gain
	Output simulated
	Output calculated
	Output buffered

V_OUT [V]

V_in [mV]

A_0 [dB]
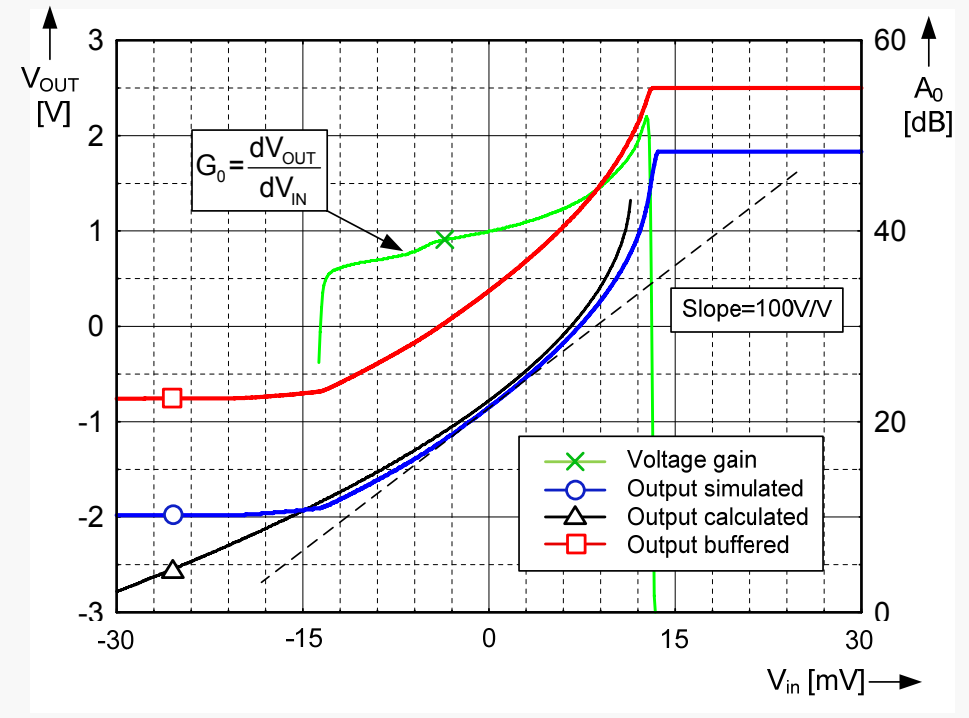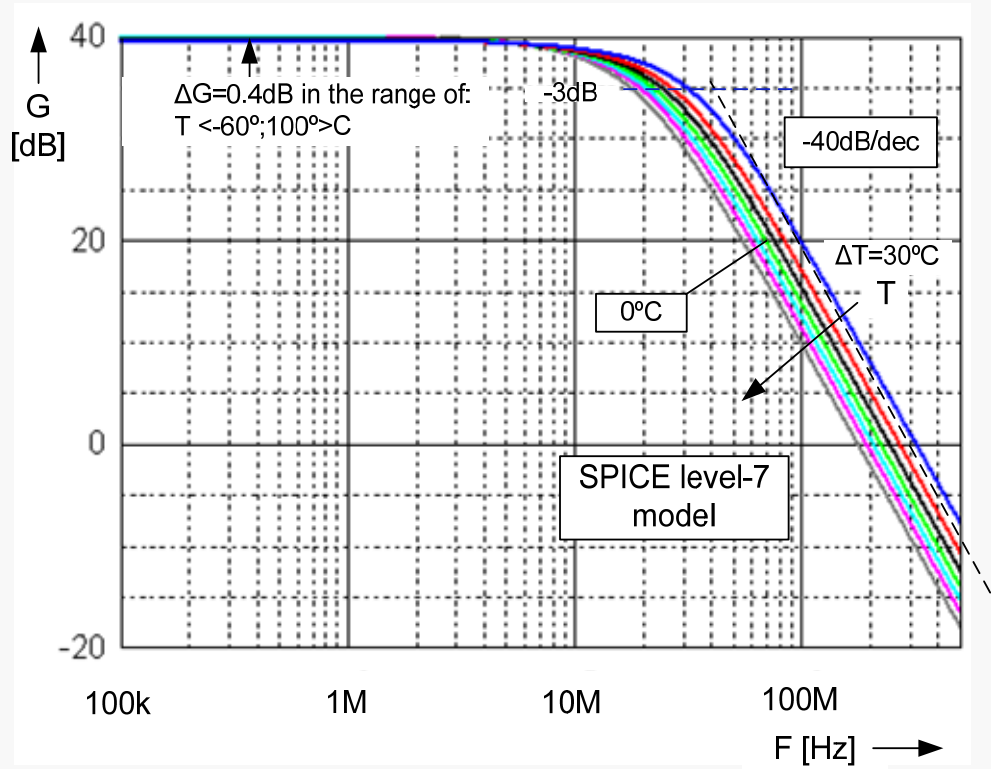
➔ Sensitivity analysis:

i) global:

$$S_{x_i}^{G_0} = S_{W_D, L_{eff}, I_B}^{G_0} = -S_{L_D, W_{eff}, I_L}^{G_0} = \frac{\partial G_0}{\partial x_i} \cdot \frac{x_i}{G_0} = \frac{1}{2}$$

i) related to bias currents: $I_B/I_L = 2/(k-1)$

$$S_k^{G_0} = \frac{1}{2} \frac{k}{k-1}$$

High I_B/I_L matching required